RMAP IP CORE

Chris McClements, Martin Dunstan
Steve Parkes

Space Technology Centre
University of Dundee

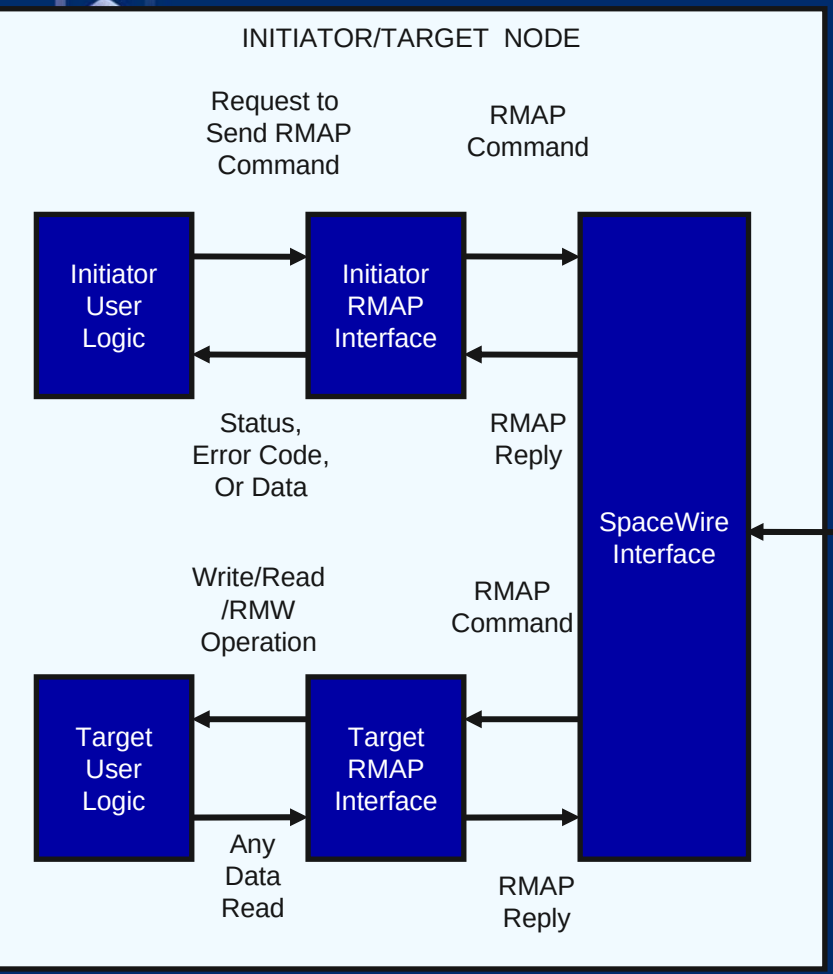
Introduction

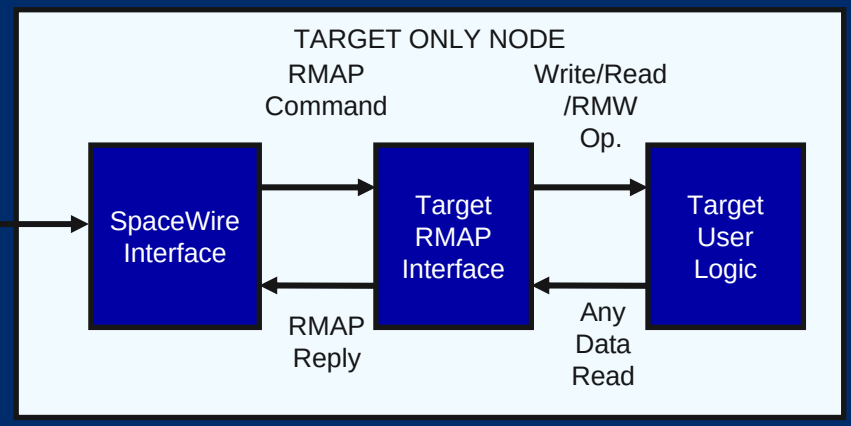
- Synthesisable VHDL model
  - IP block
  - Target only, initiator only, or target and initiator command encoder and decoder
    - Receive RMAP commands and send replies (Target)
    - Send RMAP commands and receive replies (Initiator)
  - Generic model
- Configurable at synthesis time
  - VHDL **generic** port controls all configurable elements in the IP core
  - Configurations supported through VHDL **generate** statements

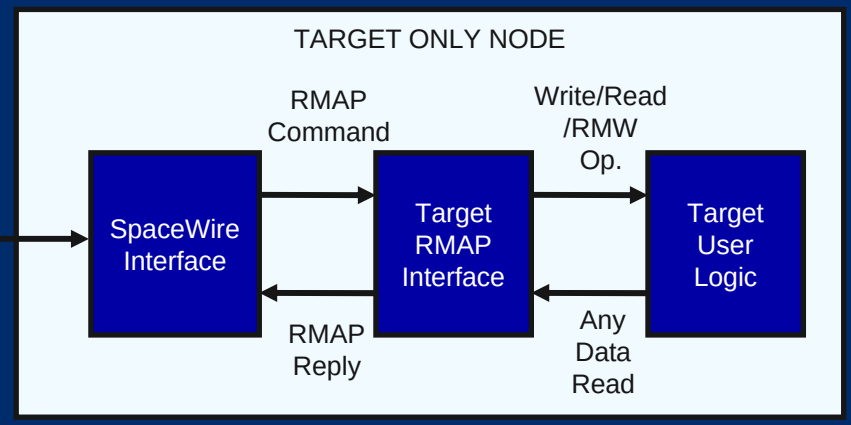
Functions

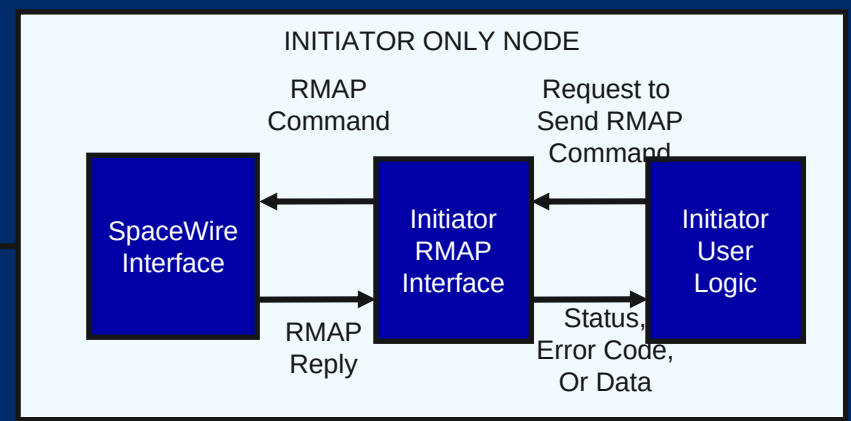
- Target
  - Decode commands to target
  - Encode target replies
  - Store verified write command data
  - Authorise target commands
- Initiator
  - Encode initiator commands (Header/Data)
  - Decode replies to initiator (Status)
  - Manage multiple commands
  - Manage commands which do not receive replies
- Indicate target/initiator status
- DMA controller. Read/write data to host bus.
  - Pipelined like AHB interface. Control phase/Data phase

System Design

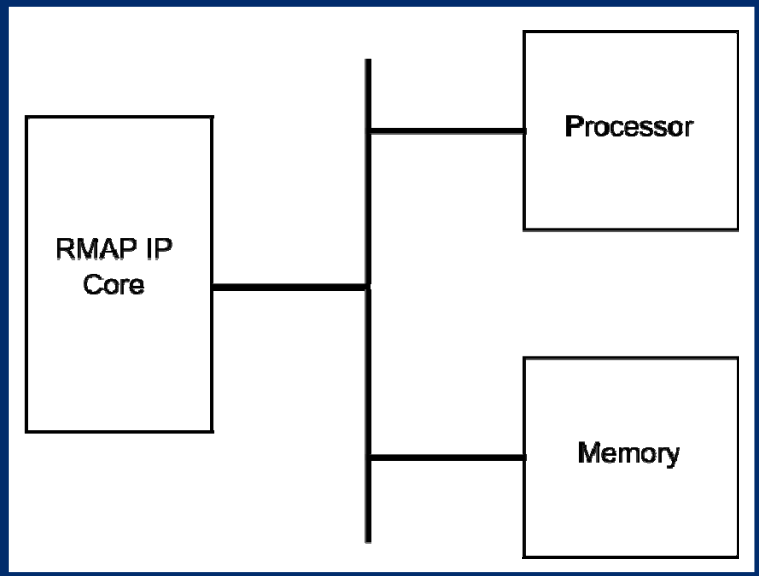








System Design



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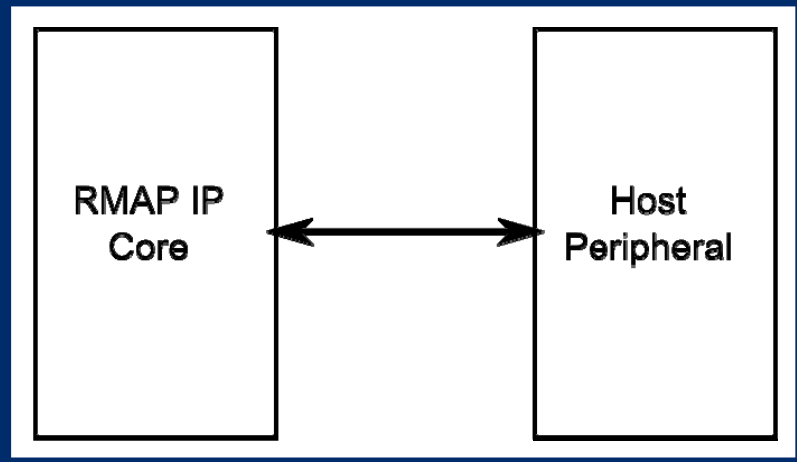

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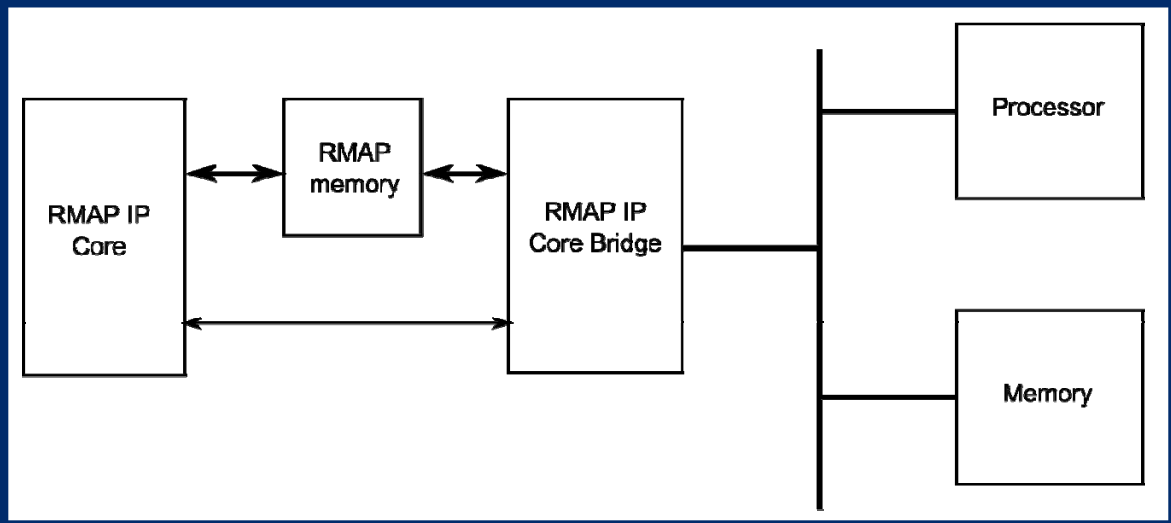

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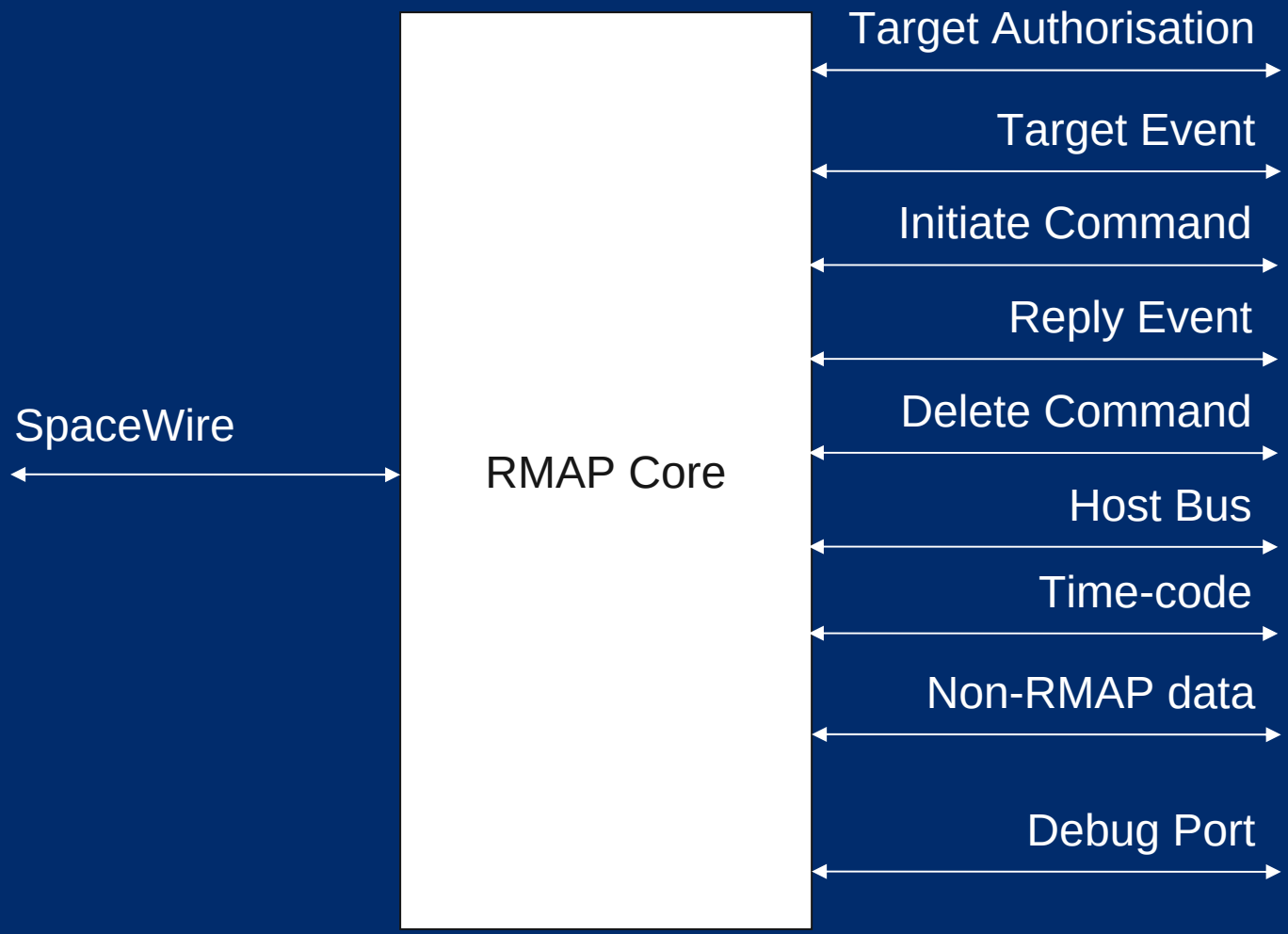
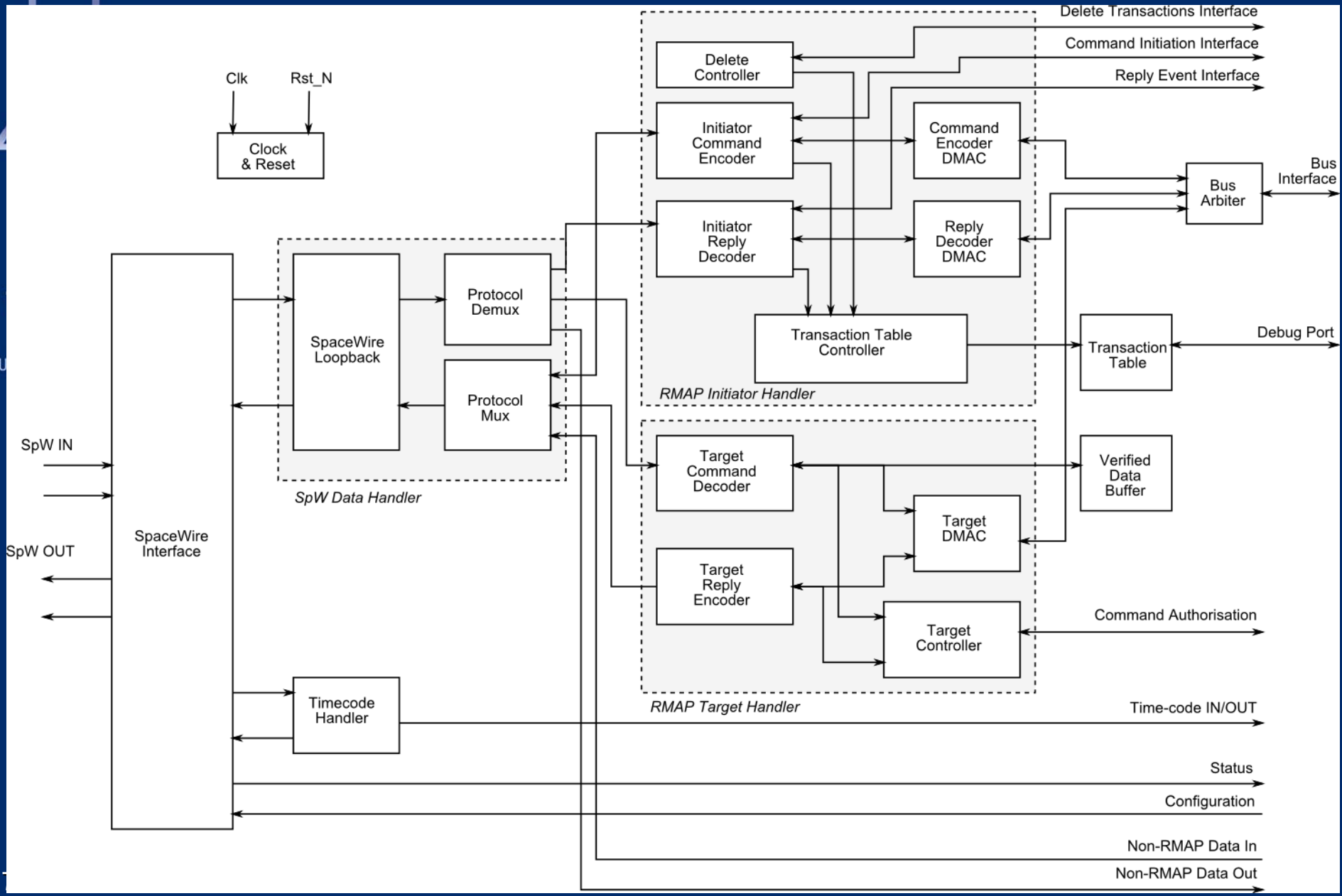
Interfaces



Architecture



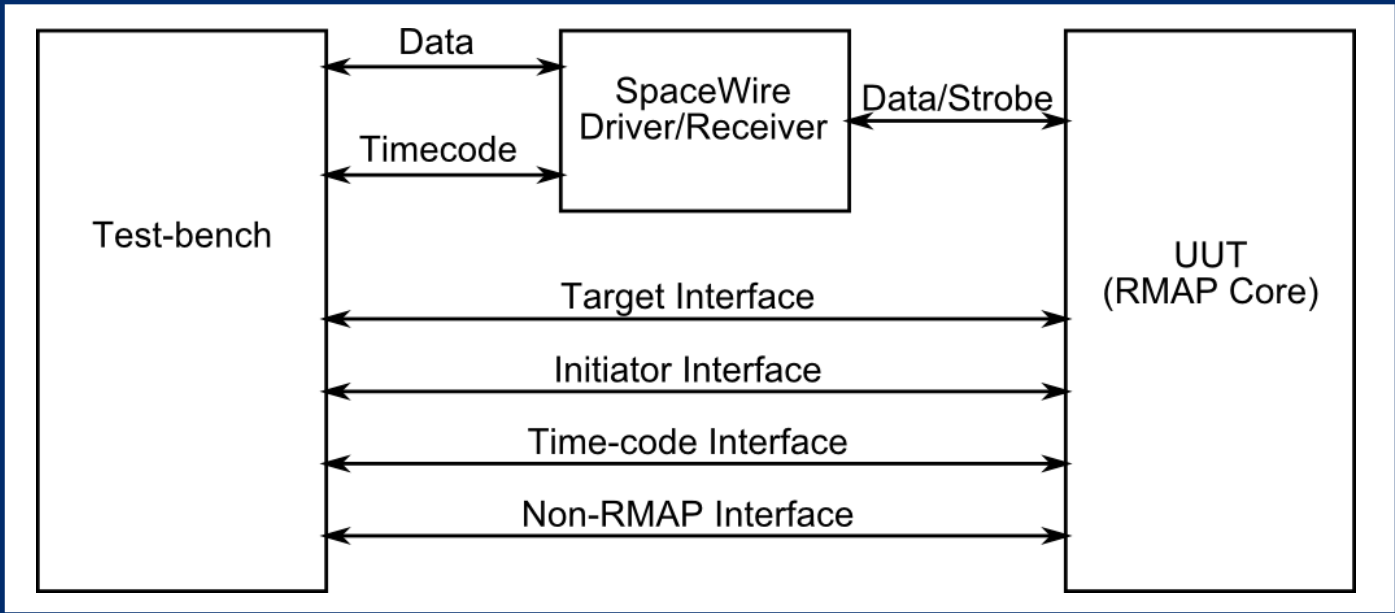
Configuration

- Target enabled.
- Initiator enabled
- External Data Bus Size (Size in bits)
  - 8, 16, 24, 32 ... 64, etc.
  - Initiator restricted to 32 bits
- Data format
  - MSB or LSB first
  - Initiator data structures, MSB or LSB first
  - Bit swapping
- Target verify buffer size
- Initiator transaction table size
- Initiator timeout detection period
- DMAC
  - Burst size
  - FIFO size
  - Watchdog

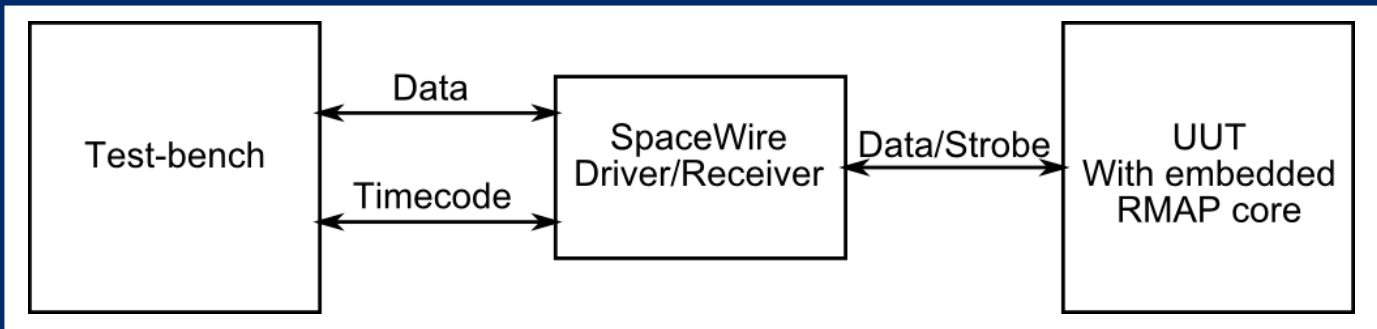
End user testing

- Two test configurations
  - End user test-bench
  - Embedded test-bench
- End user test-bench
  - Runs RMAP target and initiator tests
  - Check function of netlist or placed and routed model.
- Embedded test-bench
  - RMAP core embedded in host system
  - SpaceWire interface is only exposed external interface
  - Send and receive SpaceWire packets to the users system

End User Testing



End user test-bench



Embedded end user test-bench

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Synthesis and Implementation

- Single clock for all RMAP core operations
  - SpaceWire interface requires receive clock and may have separate transmit clock
- Area usage
  - Target and initiator and both,
    - 32 bit external bus
    - 32 word burst size
    - 64 word DMAC FIFOs.
    - 36 Outstanding Initiator Transactions
  - Synthesis results from Mentor Graphics precision tool

Model	AX2000			ProASIC3E1500	Spartan3E 1600
	FF	Comb	Modules	Tiles	CLBs
Total	3160	7530	10839 (34%)	11134 (29%)	3172 (21%)
Initiator Only	2170	5239	7489 (23%)	7856 (20%)	-
Target Only	1420	2936	4429 (14%)	4542 (12%)	-
Kernel Only	2794	6871	9824 (30%)	10039 (26%)	-

Status

- VHDL code completed
- Functional verification completed
  - RTL model in all configurations
  - Netlist model of initiator and target (Synplify and Mentor Graphics netlist)
- Documentation available
  - User manual
  - End user test-bench manual
- Initial user feedback obtained
  - Documentation update
  - End user test-bench update
- Alpha site testing on-going