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Distributed, Real-Time, Embedded Systems

MARC Mini-Project and SpaceWire-RT

SpaceWire Working Group Meeting #12

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Presented by:

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MARC Mini-Project

- SEA (H/W) & SciSys (S/W), Astrium UK (System & Demo)
  - ⇨ GSTP 2007-10

- S/W objective: specify, design and implement an onboard software framework product (GenFAS) based on the CCSDS SOIS architecture using the LEONFT2 processor and providing the applicable subset of the SOIS communications services mapped onto SpaceWire

- Current status:
  - ⇨ CDR (detailed design) for GenFAS in Mid March 2009
  - ⇨ So GenFAS detailed design not yet complete – please take account in remainder of slides

MARC Constraints (1/2)

- **SpaceWire-RT shall be used to implement SOIS QoS**
  - ⇨ Scheduled SpW-RT network only
  - ⇨ Based on Initial Protocol Definition, Issue 2.1

- **No SpaceWire-RT support in hardware**
  - ⇨ Only the RMAP and SpaceWire Codec IP cores are being used in the Core Computing Modules (CCMs)
  - ⇨ Therefore implementation of **SpW-RT** must be done in **software** “over the top” of RMAP (including using its raw packet bypass)
  - ⇨ Implementing the SpW-RT protocol traffic, e.g. flow-control, in software will have performance implications

MARC Constraints (2/2)

- **Dumb modules only support RMAP**
  - They are considered dumb in that they have no knowledge of any SOIS protocols (i.e. as implemented by SpW-RT)
  - There are two implications from this:
  - **Communication between CCM and dumb module must be using RMAP**
    - CCMs cannot use SpW-RT to communicate with the dumb modules as they only understand RMAP
    - Coms between CCMs and dumb modules must be done using the lowest common denominator, i.e. raw RMAP packets
    - Mechanism is required to allow both SpW-RT and raw RMAP packets to be sent and received by CCMs
  - **Dumb modules has no knowledge of SpaceWire-RT schedule**
    - SpaceWire-RT assumes it is the only protocol running on the network
    - Therefore the raw RMAP traffic can interfere with it
    - Dumb module has no knowledge of SpaceWire-RT
    - Therefore cannot have any knowledge of the SpaceWire-RT schedule used for synchronous communications to meet the timeliness characteristics
    - To cater for this, the scheduling of communication initiated from dumb modules needs to be managed so that they do not interfere with or are explicitly catered for into the SpaceWire-RT schedule.

Agreed Tailoring of SpaceWire-RT (1/2)

- Only Basic, Best-Effort, Assured and Reserved QoS
  - ⇨ no requirement for Guaranteed QoS
- No redundancy
  - ⇨ redundancy is handled by FDIR by switching plane through updating Routing Tables rather than internally by SpaceWire-RT
- No Group Adaptive Routing
  - ⇨ remove likelihood of out of sequence packets and subsequent retries – therefore Basic and Best-Effort have in effect the same QoS
- No priority for Reserved QoS
  - ⇨ not necessary – this is being fed back to the SOIS WG itself

Agreed Tailoring of SpaceWire-RT (2/2)

- Packets with Best-Effort and Assured QoS will be scheduled for sending using the "Allocated" mechanism
  - ⇨ the "opportunistic" mechanism will not be implemented - so as to be more predictable & simpler mechanism

- API will be the Memory Access Service (using RMAP) and the Packet Service (using SpW's CCSDS Packet Transfer Protocol)
  - ⇨ the "stream interface" will not be implemented as it creates unnecessary complications between the SpW-RT "core" and the Memory Access and Packet Services

- Flow control is be implemented so as to investigate suitability and to allow in future for interoperability
  - ⇨ however the source and destination channel buffers will be sized to maximum SDUs not a stream API

Variations from SpW-RT for MARC

- Raw channels introduced with Best-Effort QoS
  - ⇨ to **bypass** SpaceWire-RT **encapsulation** but remain within SpW-RT time-slot schedule
- Raw time-slot introduced
  - ⇨ may be considered similar to Master time-slot but allows for one or more packets from Raw channels to be sent, fitting into the schedule in an “allocated asynchronous” manner
- Priority is a configuration parameter of a Best-Effort or Assured channel, not encoded by channel number
  - ⇨ so as to allow more than one channel between same source and destination with the same priority level
- No prioritisation within a “scheduled timeslot”
- Channel buffers organised as an SDU FIFO not as a byte FIFO
  - ⇨ as this is the interface required by higher level software
- Proposing to change BFCT packet to use 4 bits for destination buffer status
  - ⇨ see next slide - allows larger buffer to be managed
- No Kill mechanism

Concerns with SpW-RT (1/2)

- Flow Control
  - ⇨ Flow Control is too complex – why not just discard packet at destination if buffers are full?
  - ⇨ Flow Control in software is SLOW
  - ⇨ Destination must know SpW-RT schedule from source so as to generate BFCT packets
  - ⇨ BFCT packet only allows for signalling of space for up to 3 maximum DPs (768 bytes) which is too small for many SDUs (a sensible max SDU is 1K) and even then only one SDU

- Acknowledgements
  - ⇨ Why not done at the end of same timeslot where packets sent?
  - ⇨ Not clear how to indicate less that 6 acknowledgements in an ACK packet
  - ⇨ Not clear how to restart Assured channel after dropped packets, cannot "reset" sequence count

Concerns with SpW-RT (2/2)

- Scheduling
  - ⇨ Must all reserved channels in a time-slot be to the same destination?
    - ↳ If so, why?
  - ⇨ Scheduling mechanism prevents true asynchronous because only allow sending Best-Effort/Assured channels from a source to a single destination within an “allocated” time-slot
  - ⇨ Configuration of channels and schedule tables not defined
  - ⇨ No method for distributing schedule tables
  - ⇨ Offline tool required to generate node schedule tables and/or cross-check to ensure no resource clashes
- Channel for RMAP Reply Packets
  - ⇨ Channels are uni-directional
  - ⇨ So which channel does RMAP Target use for RMAP reply packets?
- SpW-RT does not address SOIS Synchronisation Service
  - ⇨ In MARC, time-codes also used for SCET ticks
  - ⇨ Potential conflicting frequency for SCET ticks and SpW-RT time-slots