ESA IP Cores Service

SpaceWire –related updates and developments

Kostas Marinis (TEC-EDM / ESTEC)

Kostas.Marinis@esa.int

Chris McClements (University of Dundee)

cmcclements@computing.dundee.ac.uk

Agenda

- Overview of the ESA IP Cores Service
- SpW –related updates and additions to the ESA IP Cores catalogue
- Overview of the SpaceWire RMAP IP core [by UoD]

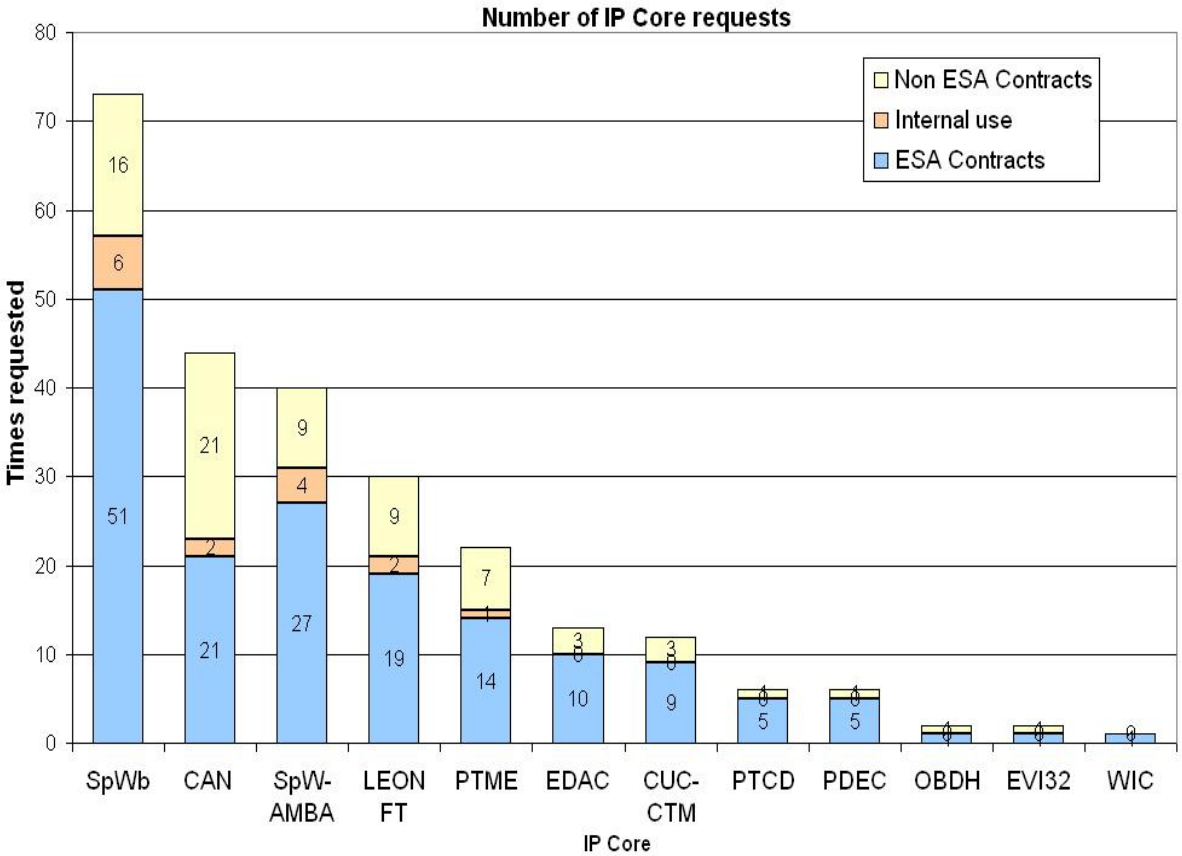
ESA IP Cores Service

- The Microelectronics Section (TEC-EDM) in ESA/ESTEC maintains and distributes under ESA licenses a catalogue of reusable building blocks (*IP Cores*) in HDL format (VHDL) which comprise typical digital functions used in space applications (SpaceWire, CAN, LEON2-FT, TM/TC, EDAC, etc).
- These IP Cores were developed in the scope of European Space Agency (ESA) activities
  - Ranging from in-house developments to contractor work, and from simple Field Programmable Gate Arrays (FPGA) to complex System-On-a-Chip (SOC) devices.
- ESA IP cores are "soft-cores", i.e. technology independent.
  - Can be synthesized and targeted to any ASIC or FPGA technology.

ESA IP Cores Service

- **ESA/ESTEC provides this "IP Cores" service as an attempt to:**
  - Counteract obsolescence and discontinuity of existing space standard ASICs, thus helping to guarantee the availability of some key functions in a technology independent format ("soft format").
  - Reduce costs of large IC developments (e.g. Systems-on-Chip) by re-using already designed and validated IC functions.
  - Facilitate the reuse of results from TRP/GSTP programs
  - Promote and consolidate the use of standardized functions, protocols and/or architectures (e.g. SpaceWire, CAN, TM/TC, etc).
  - Centralize IP users' feedback to improve quality of existing IPs and identify future needs.

ESA IP Cores Service



(*) statistics for period 04/2002 – 01/2009

- ✓ Deliverables with each IP core:
  - ❖ Documentation
  - ❖ VHDL source code
  - ❖ Testbenches
  - ❖ Simulation and synthesis scripts
- ✓ Documents can be downloaded from the IP cores website
- ✓ Precompiled simulation model available upon request (for evaluation purposes; no license required)
- ✓ Details and information on the TEC-EDM website (ESA IP core webpages):
  http://www.esa.int/TEC/Microelectronics/

- **Updates and additions to the ESA IP cores catalogue (planned):**
  - SpaceWire RMAP IP core
    - Currently under development by the University of Dundee
    - Based on SpaceWire-b CODEC IP core
    - Additional validation and x-checking activities internally at ESTEC
    - Expected public release on **May 1st, 2009**
    - Same licensing terms and conditions will apply as for the SpW-b CODEC (ESA funded activities only)
  - SpaceWire-b v2.03
    - New SpW CODEC release
    - Currently under review at ESTEC
    - Public release planned for **April 1st, 2009**

- **Updates and additions to the ESA IP cores catalogue (planned) – cont'd:**
  - SpaceWire CODEC in Actel RTAX FPGAs
    - Guidelines for implementing the CODEC in Actel RTAX FPGAs (synthesis constraints, P&R guidelines, etc)
    - Sample implementation, fully documented
    - Based on SpW-b v2.03, hence also available for public release on **April 1st, 2009**
    - Available to all licensed users of the SpaceWire-b IP core
  - SpaceWire RT IP core
    - Future planned development, to be included in the ESA IP cores portfolio

All announcements shall be made via the ESA IP cores website, plus via dedicated emails to all licensed users.