

Highly accurate time synchronisation through SpaceWire

Current SpaceWire Time-Code distribution

- The SpaceWire defines “Time-Code” to transmit time reference
- A Time-Code transmission request will occur asynchronously from the transmitted character stream.
- The delay between the Time-Code request and its transmission depends on the time left for the transmission of the current character.
- The delay difference between the best and the worst cases is **13 transmission bit periods**

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Improvement Proposal

- How to improve this figure ?
- Principle is to send along with the initial Time-Code its transmission delay to the receiver
 - This transmission delay is sent by the mean of a second Time-Code (**jitter-correction Time-Code**)
 - The destination node takes into account this delay to create a synchronisation signal with a fixed delay with respect to initial Time-Code request (Tick-In rising edge)

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Improvement Proposal requirements (character level)

➤ On the transmitter part:

- When a high resolution synchronisation is needed a jitter-correction Time-Code must be sent **just after the initial Time-Code**.
- This jitter-correction Time-Code is built as follow:
 - the two control flags are set to one of the remaining reserved states (TBD).
 - The four lowest bits are set to the delay M (in number of transmitted bits) between the Tick-In signal assertion and the transmission of the first data-control flag bit of the initial Time-Code.
 - The two left bits are set to zero.

➤ On the receiver part:

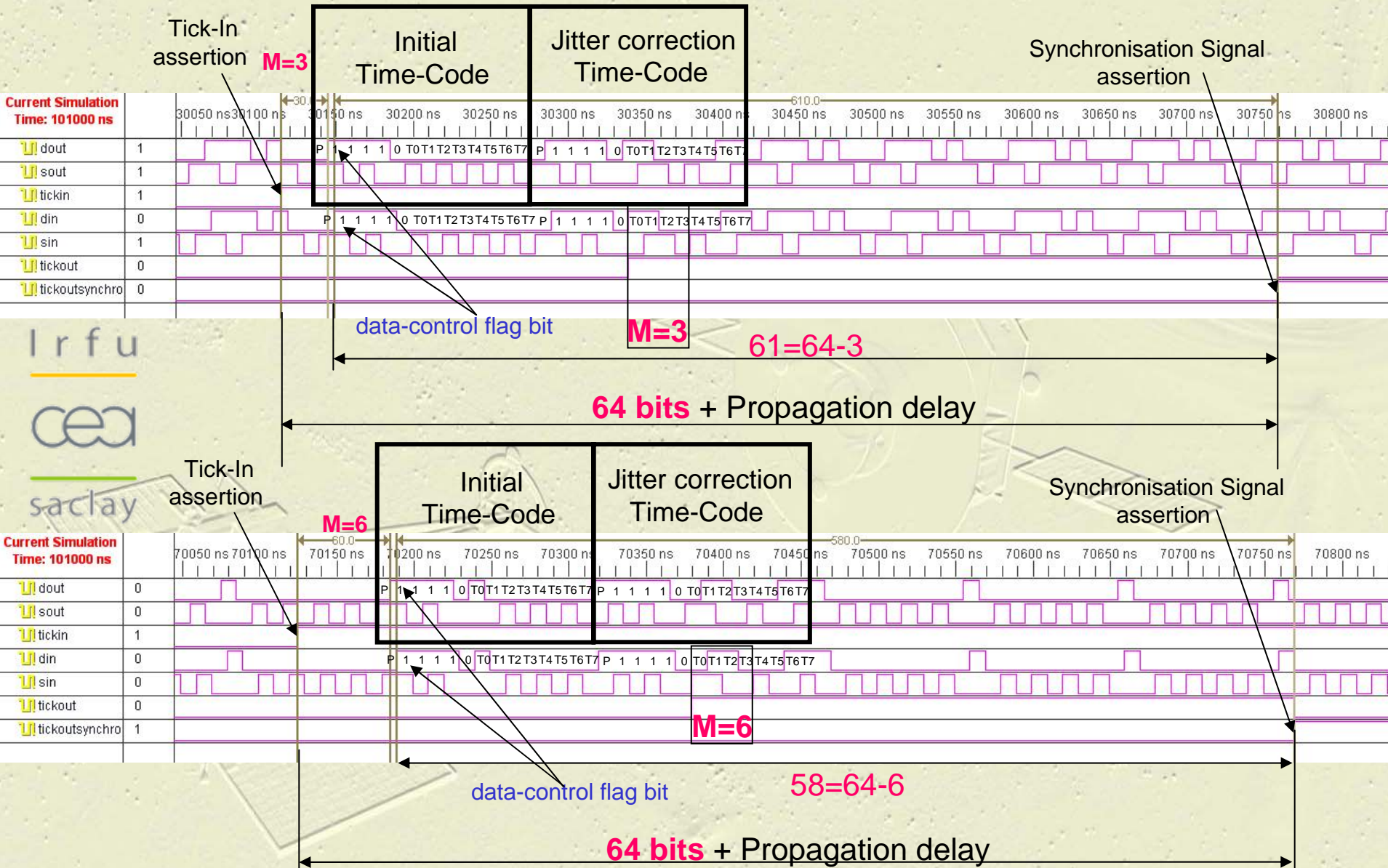
- A synchronisation signal shall be asserted after a number (64 minus M) of receiver bits from the reception of the first data-control flag bit of the initial Time-Code.

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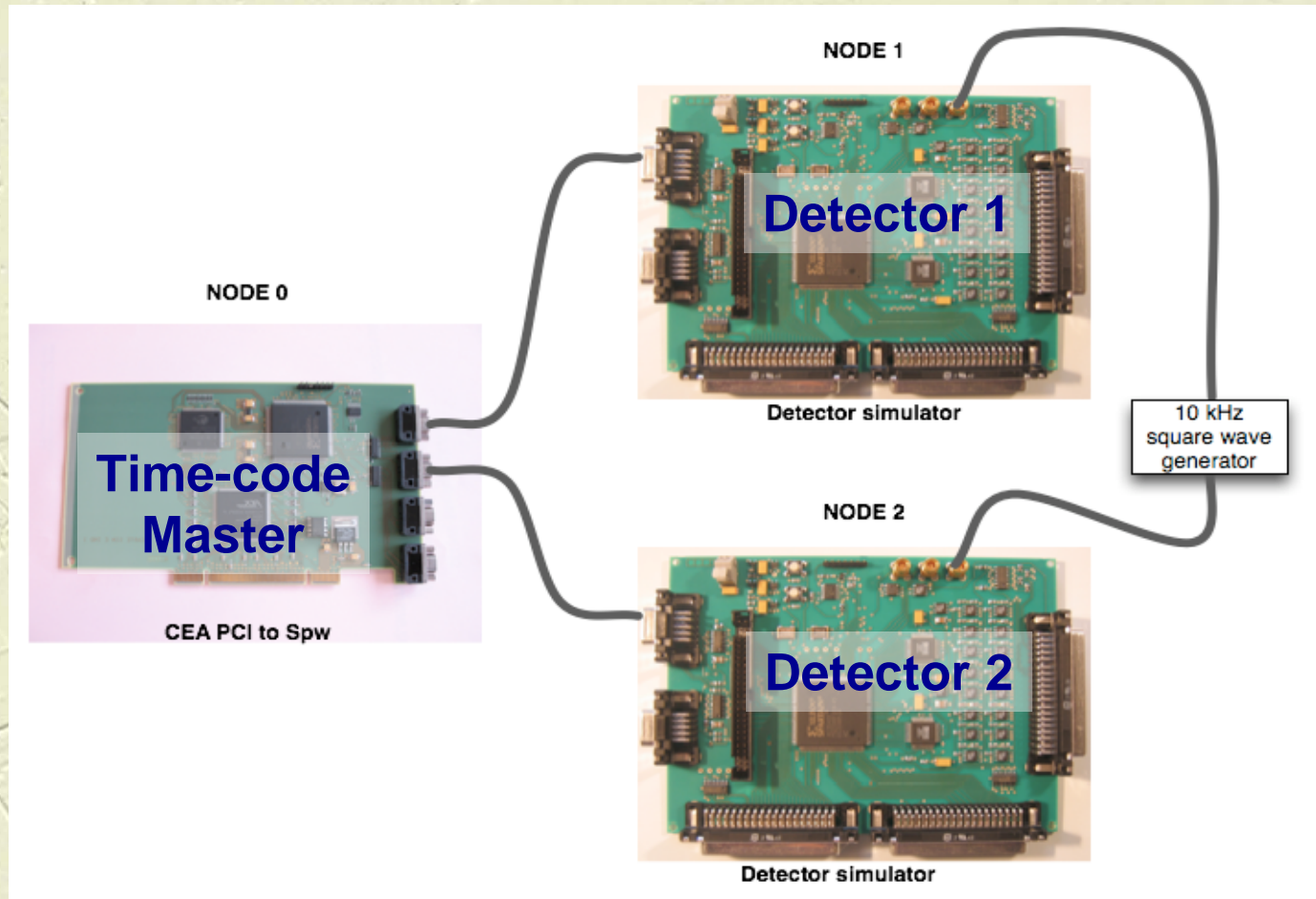
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Simulation examples:

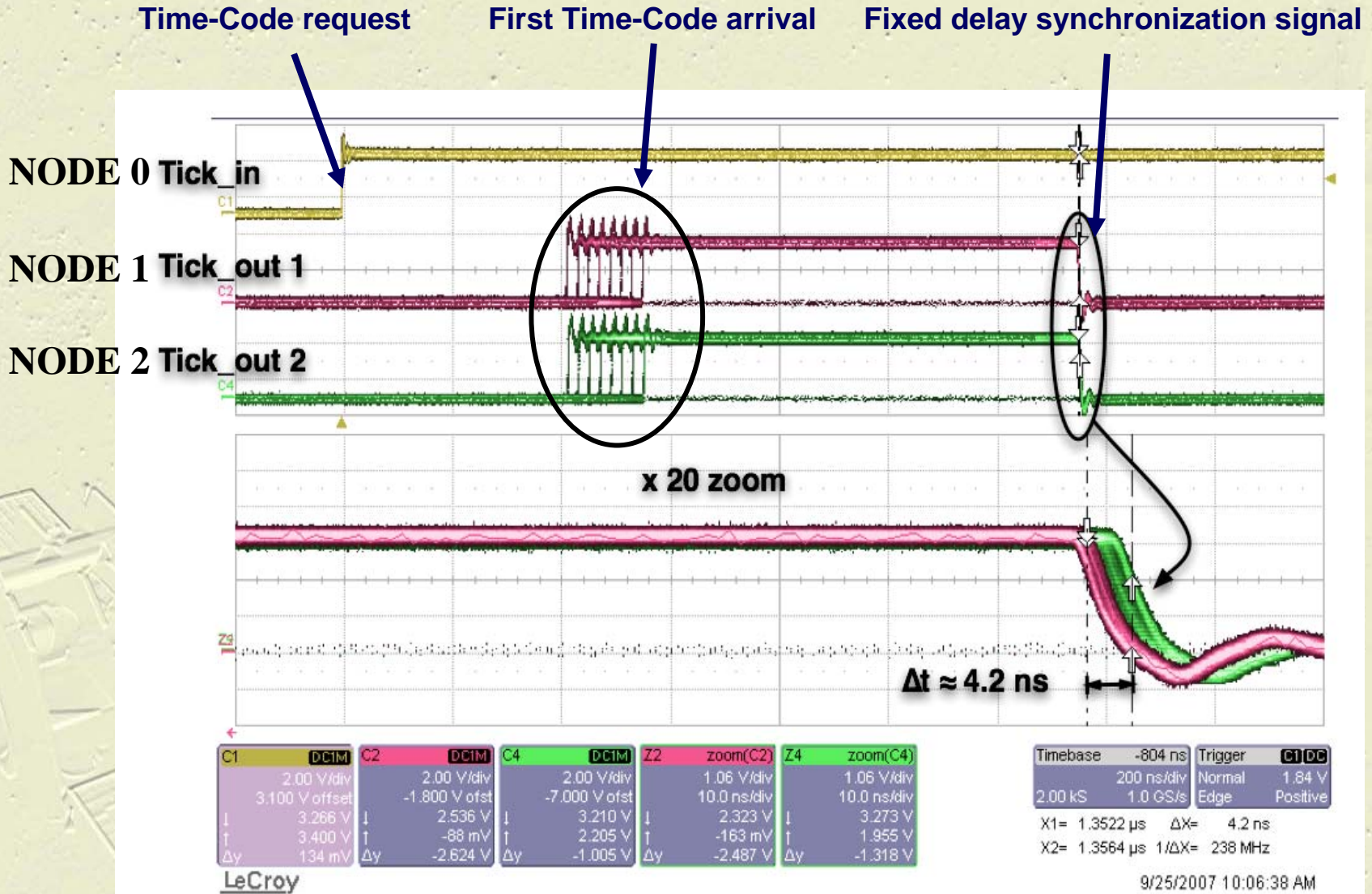


Experimental setup

- A PCI / SpaceWire board simulates the Time-Code Master while 2 detector acquisition boards simulate the destination nodes



Experimental result



SpaceWire Time-Code improvement implementation

➤ Two new functions are added to the current SPACEWIRE codec:

- One for the time transmission (TIME_TX)
 - Get Time-Code transmission delay
 - Send successively 2 Time-Codes
- One for the time reception (TIME_RX)
 - Computes compensation delay
 - Generates sync signal after compensation delay

➤ Implementation is **low resource consuming**:

- In an ACTEL RTSX-SU72 FPGA:
 - Combinational cells: 62 of 4024 (1.5%)
 - Sequential cells: 42 of 2012 (2%)

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Network aspect

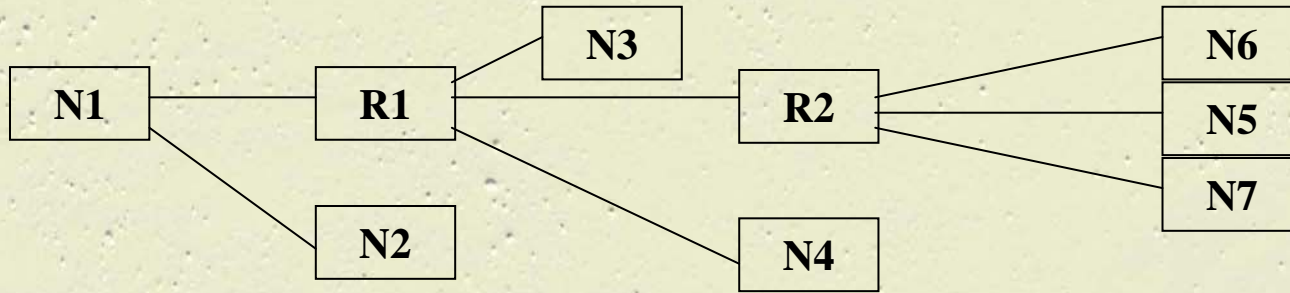
- For a highly accurate synchronisation through a SpaceWire Network
 - The same Time-Code distribution rules shall be followed
 - But a valid Time-Code is transmitted on the signal synchronization edge
 - So the delay between the time master tick-in generation and the node synchronization signal assertion dependant on the number links between them.

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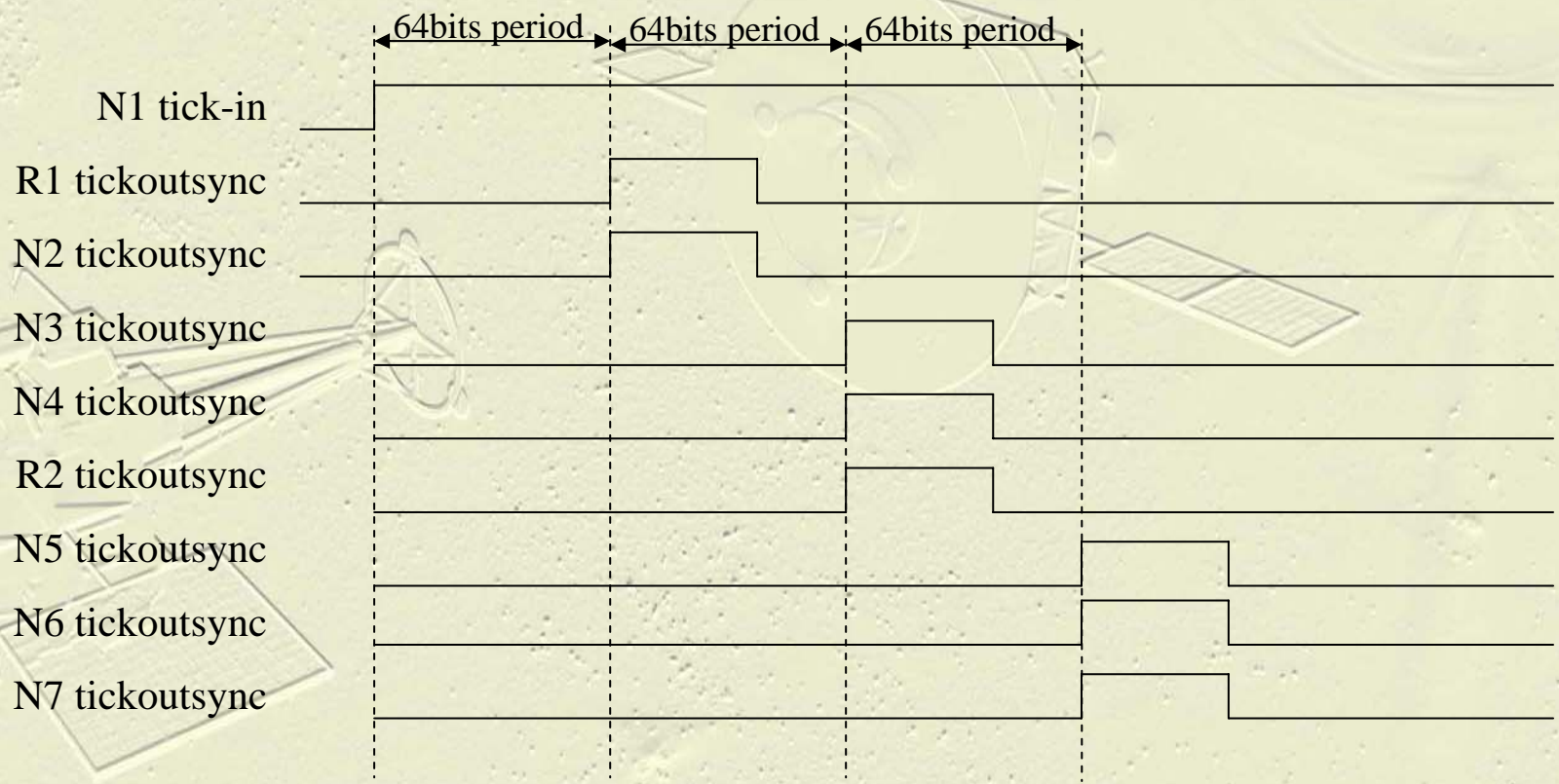
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Network example



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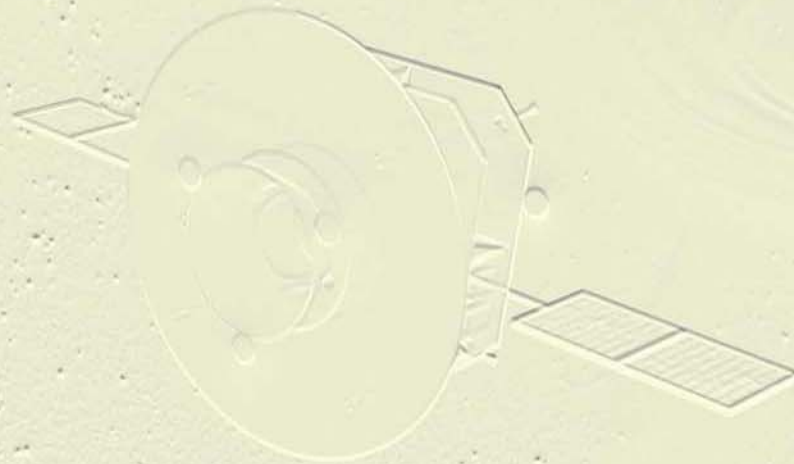
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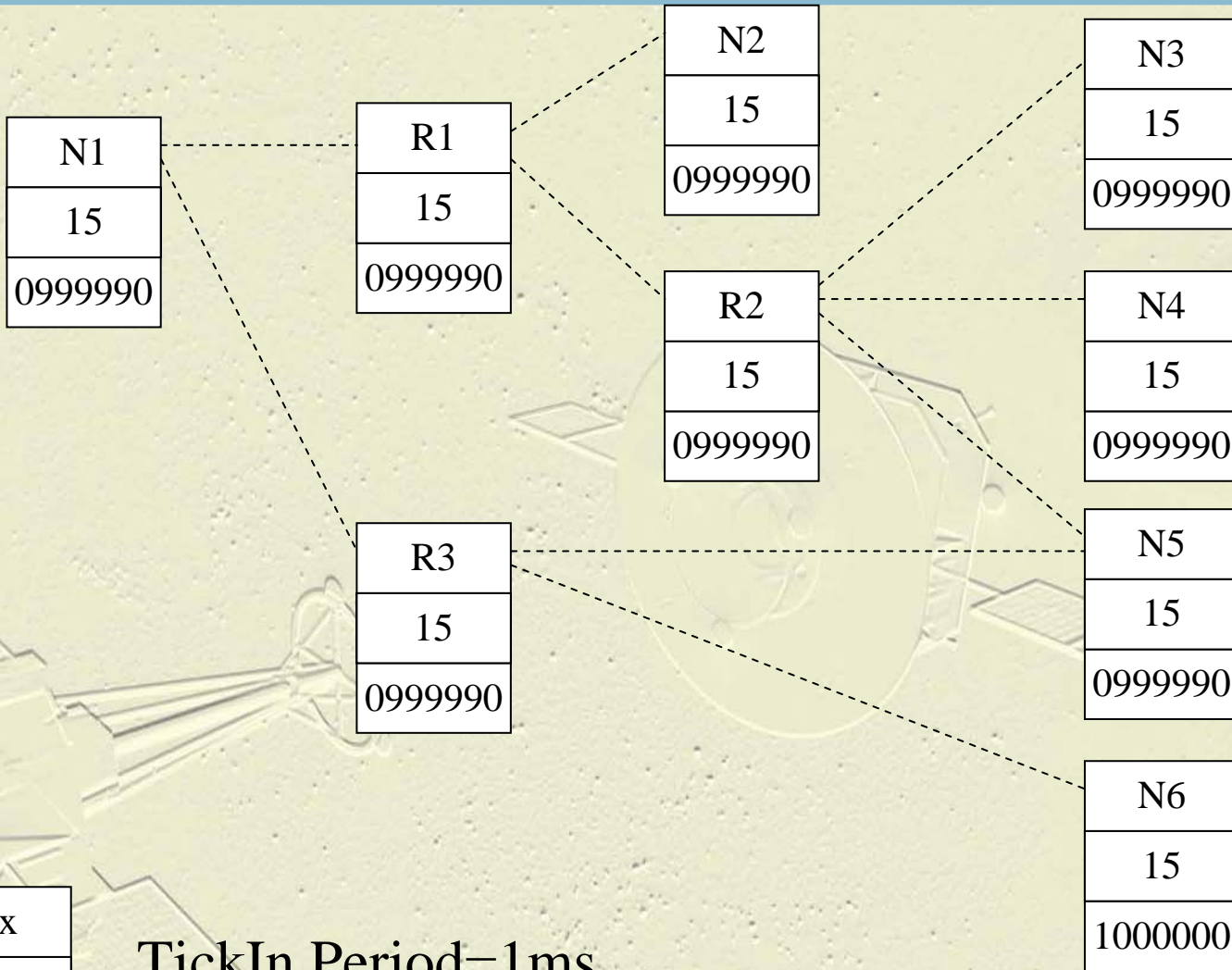
Questions & Comments

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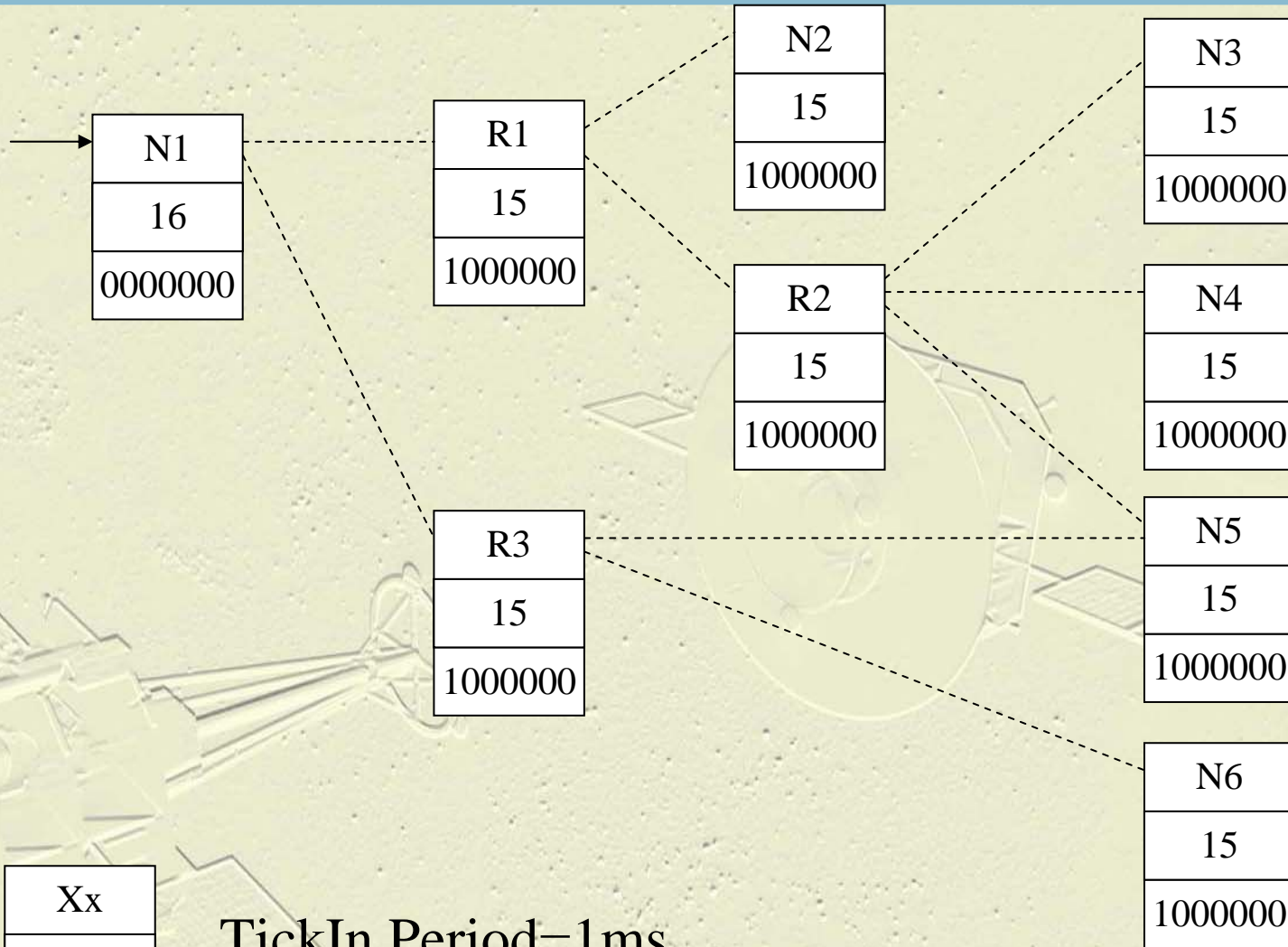


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Xx
TimeOut
SubTime

TickIn Period=1ms

Transmission Period=10ns / Links delay = 640ns

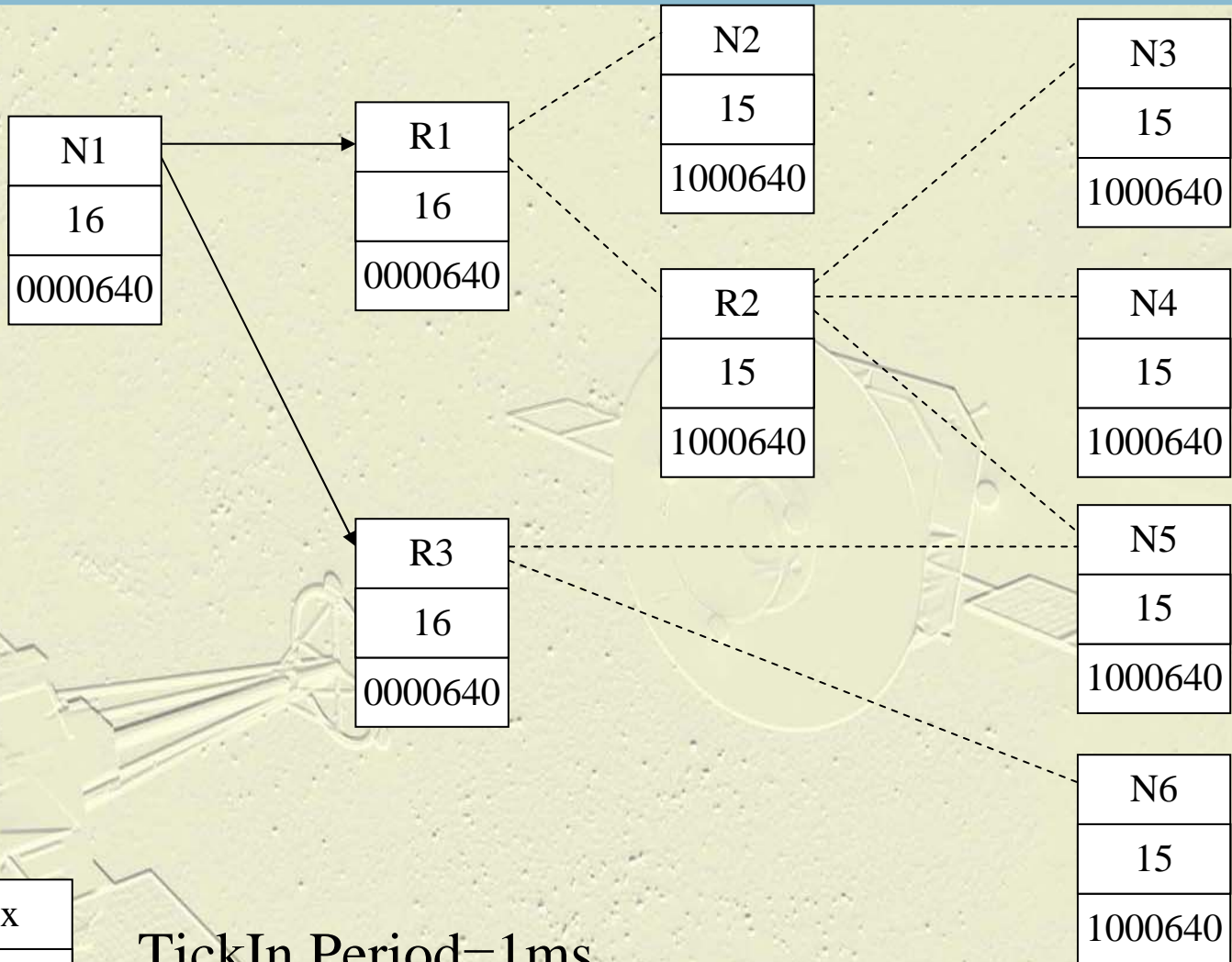


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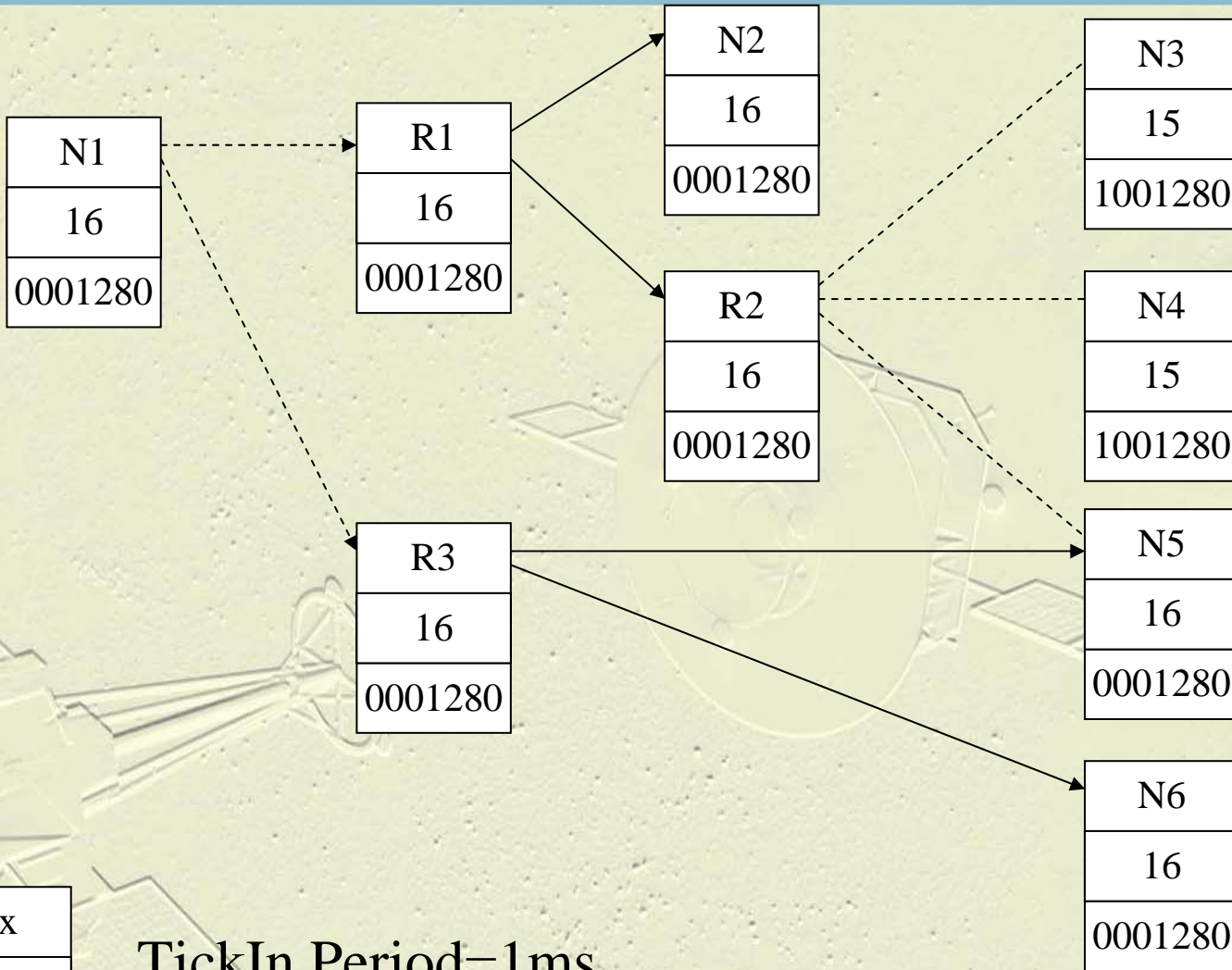


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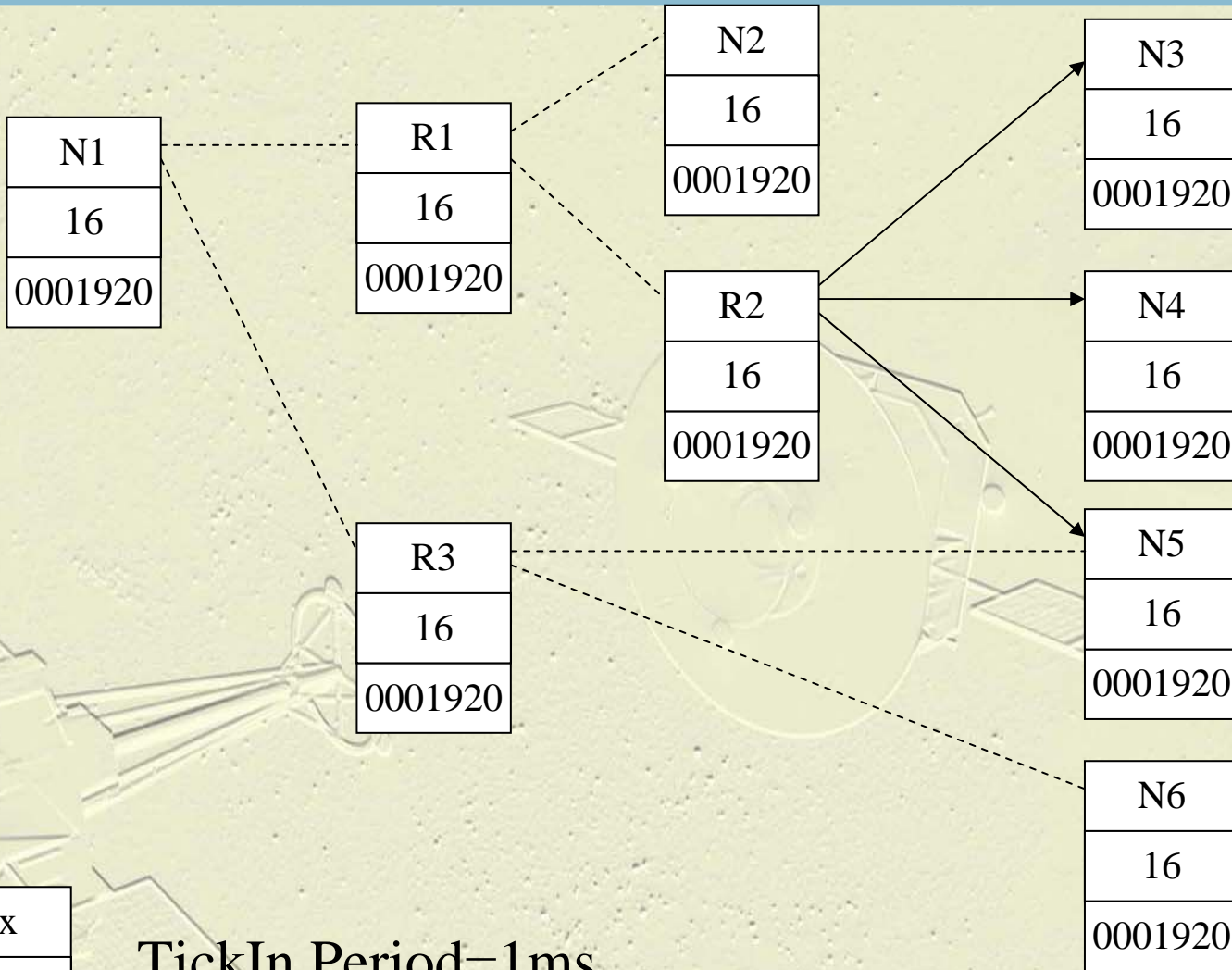


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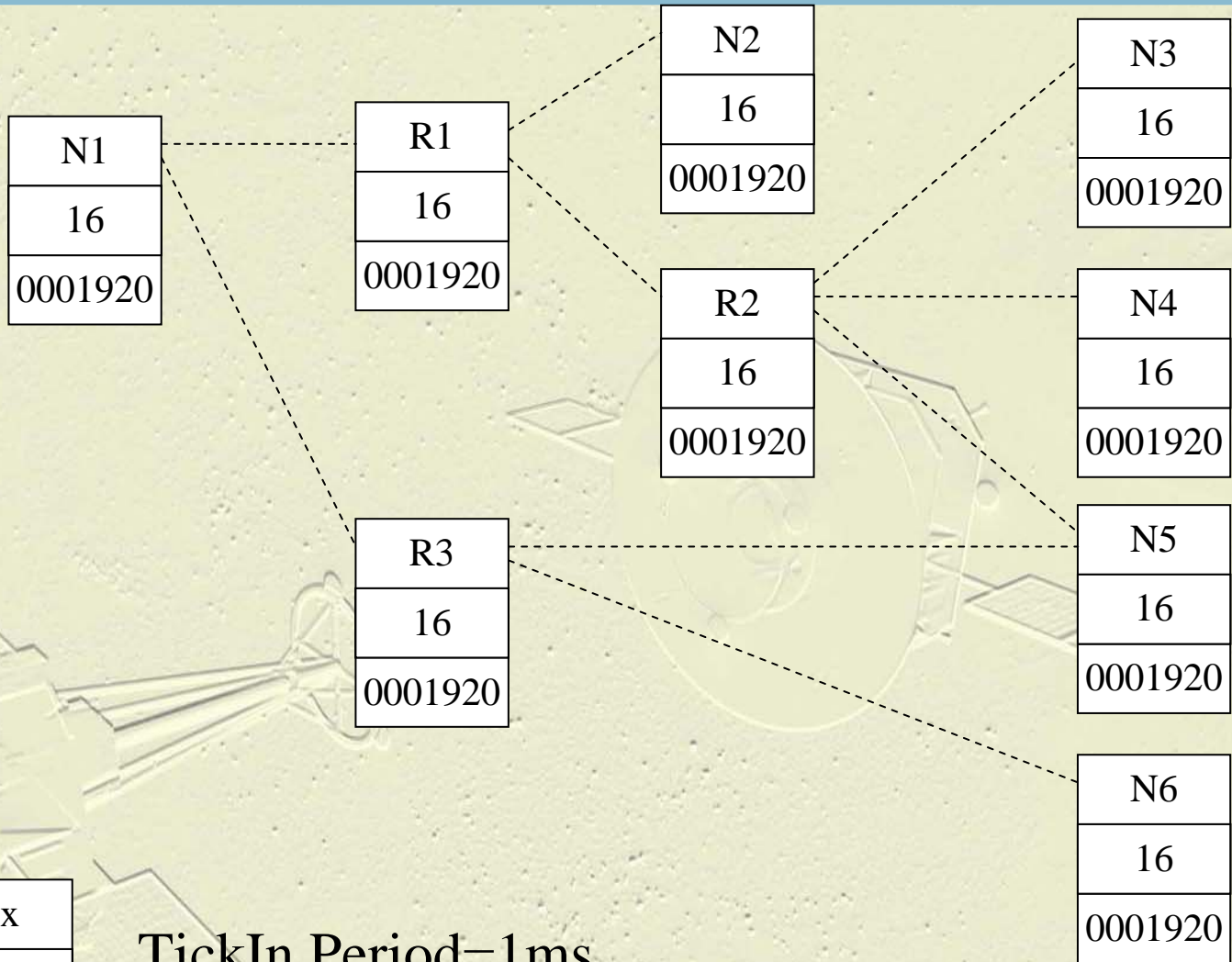
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