Test and Verification of SpaceWire Developments and VLSI Implementations.

Some Methodology and Tools

Yuriy Sheynin, Elena Suvorova, Irina Lavrovskaya

Institute for High-Performance Computer and Network Technologies
St. Petersburg State University of Aerospace Instrumentation
sheynin@aanet.ru

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Testing and verification

- Specification and verification of SpaceWire protocols
- Testing and debugging SpaceWire VLSI implementations
- Testing and debugging SpaceWire implementation products: chips and boards

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Standardized procedures?

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  SDL specification
- Testing and debugging SpaceWire VLSI implementation
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  Set of BFMs and Nest generators
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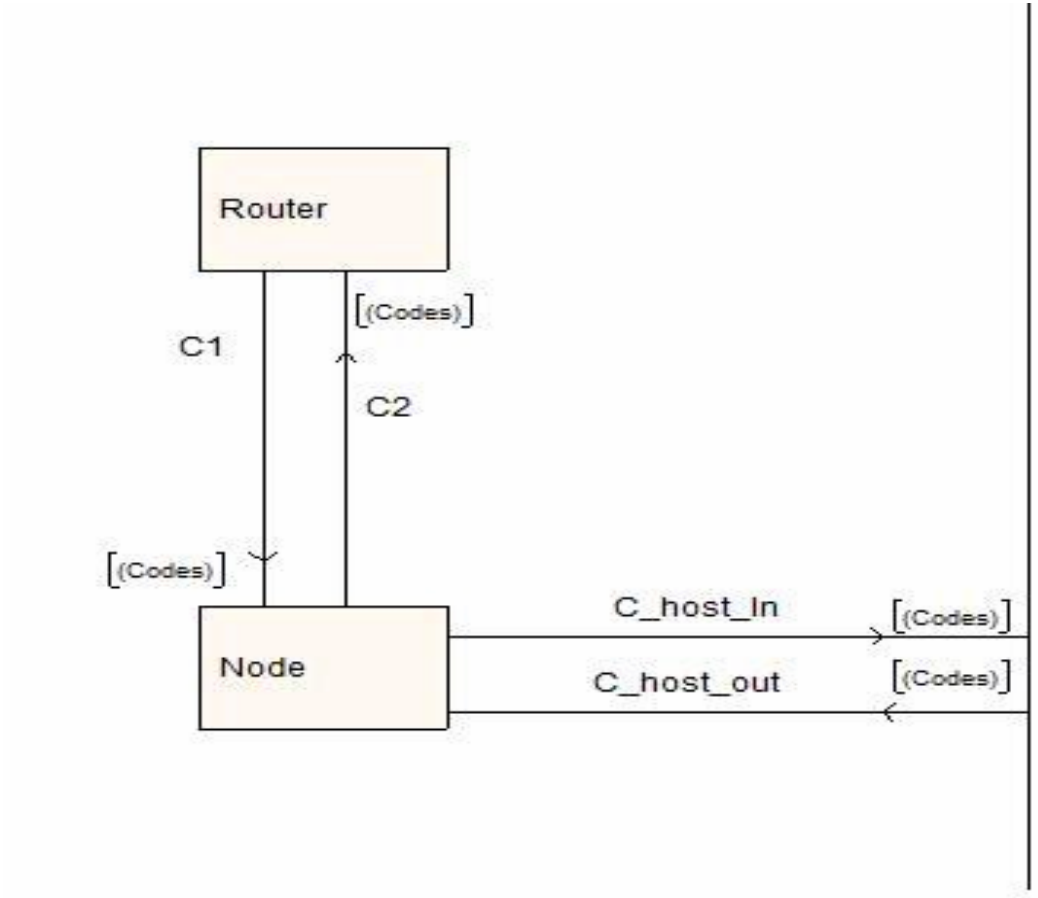
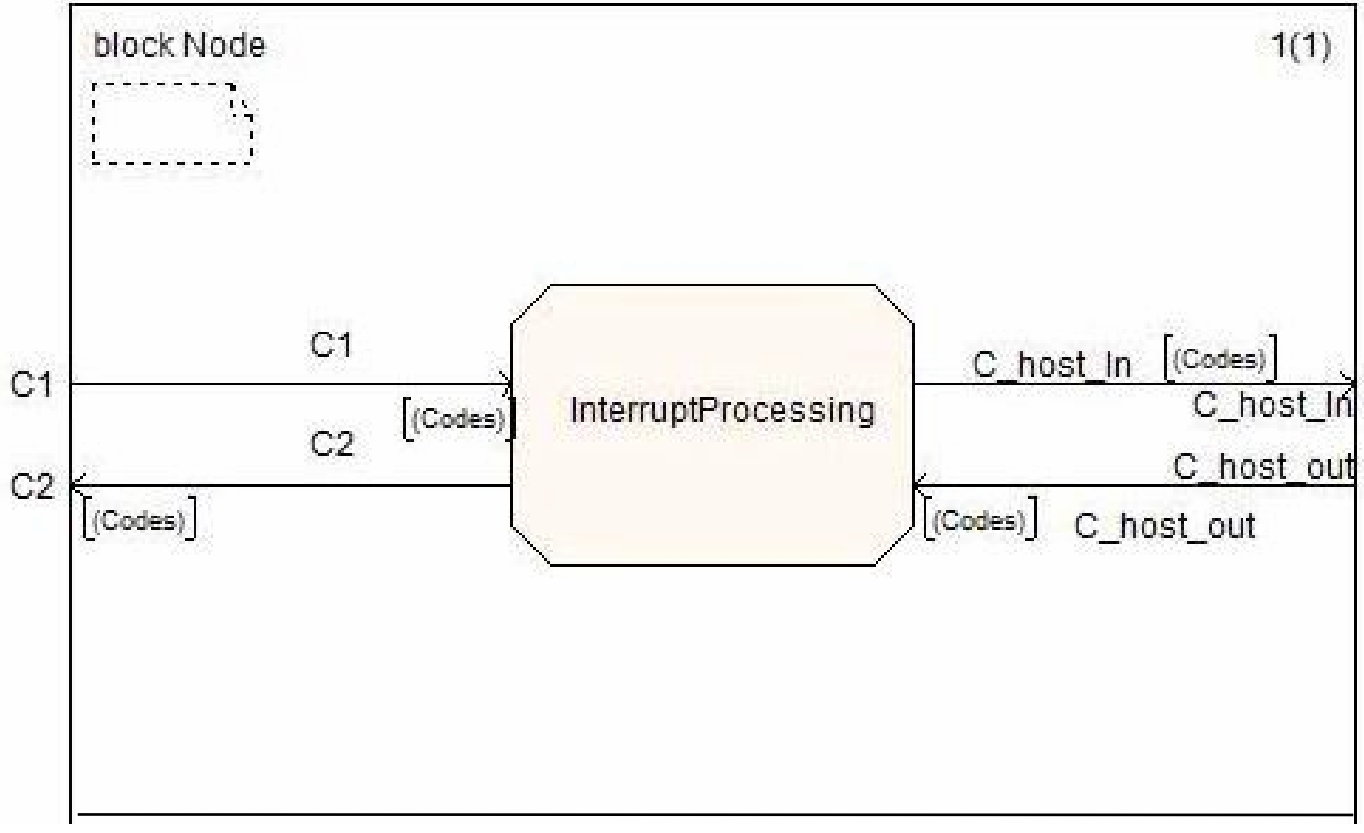
  SDL specification
  – ***SDL specification for Distributed interrupts as an example***
- Testing and debugging SpaceWire VLSI implementation
  Set of BFMs and Test generators
- Testing and debugging SpaceWire implementation products: chips and boards

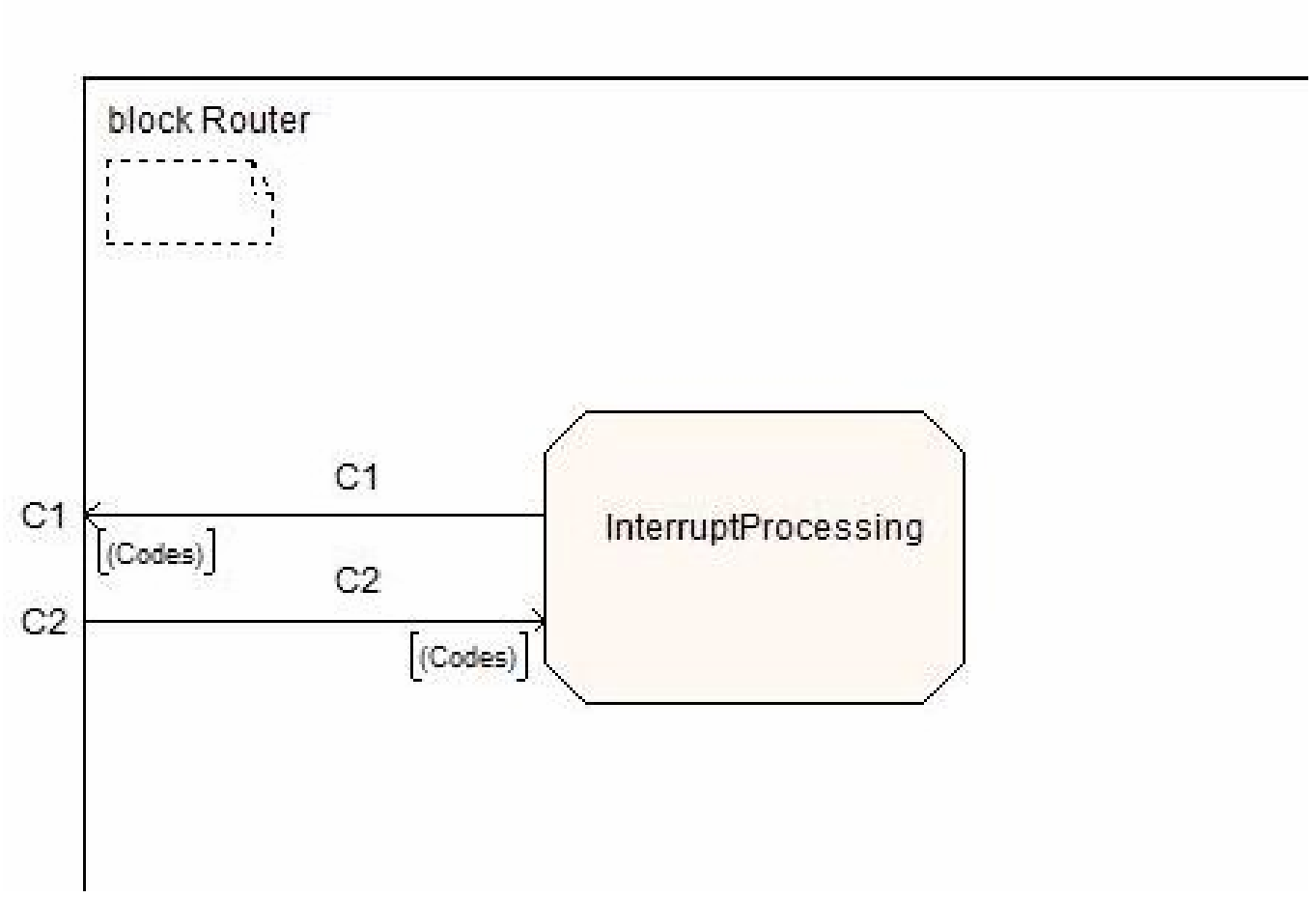
System consists of two types of blocks: Node and Router



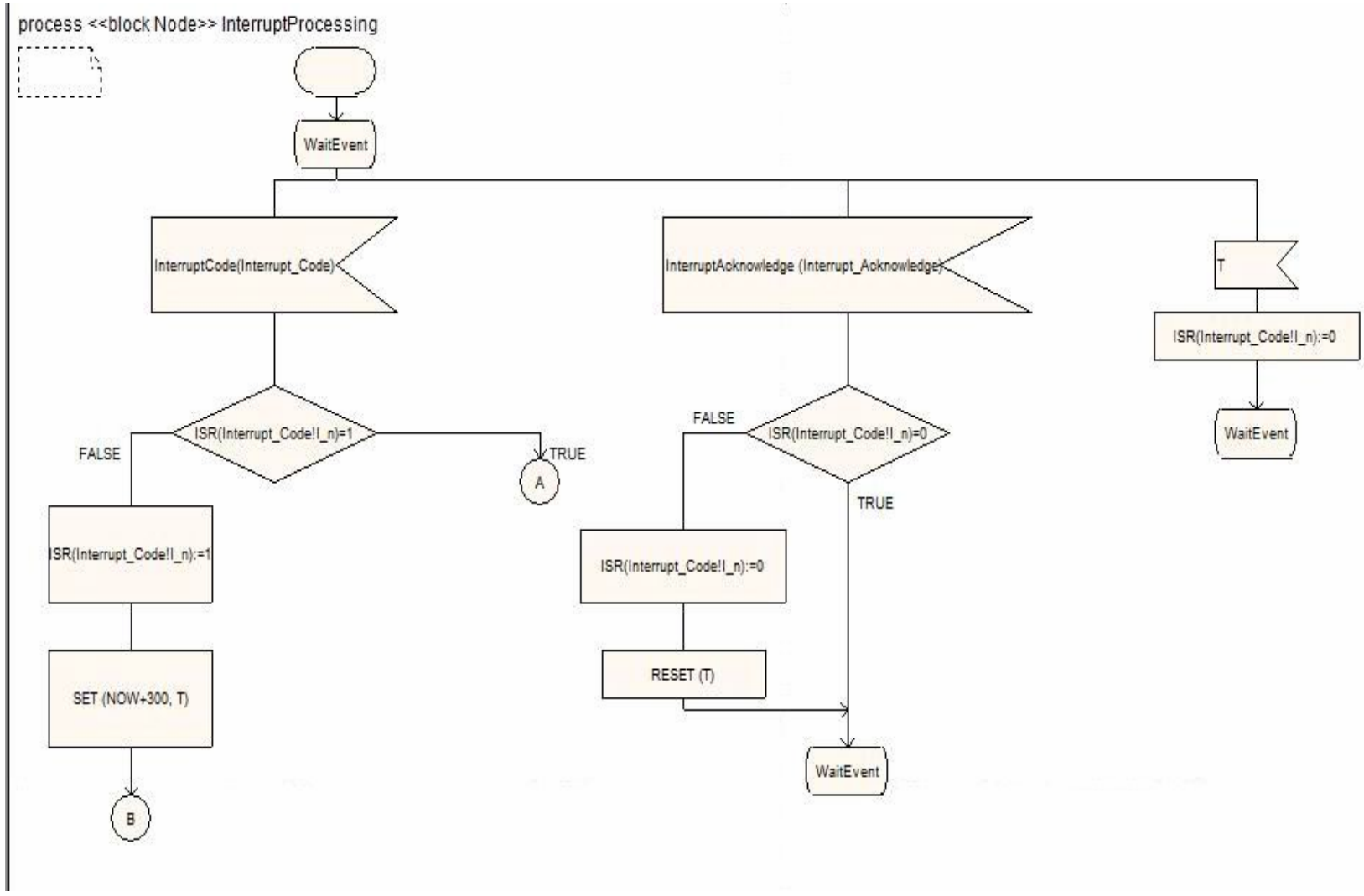
Node:


block Node
1(1)
C1
C1
[Codes]
InterruptProcessing
C_host_In
[Codes]
C_host_In
C2
C2
C_host_out
[Codes]
[Codes]
C_host_out

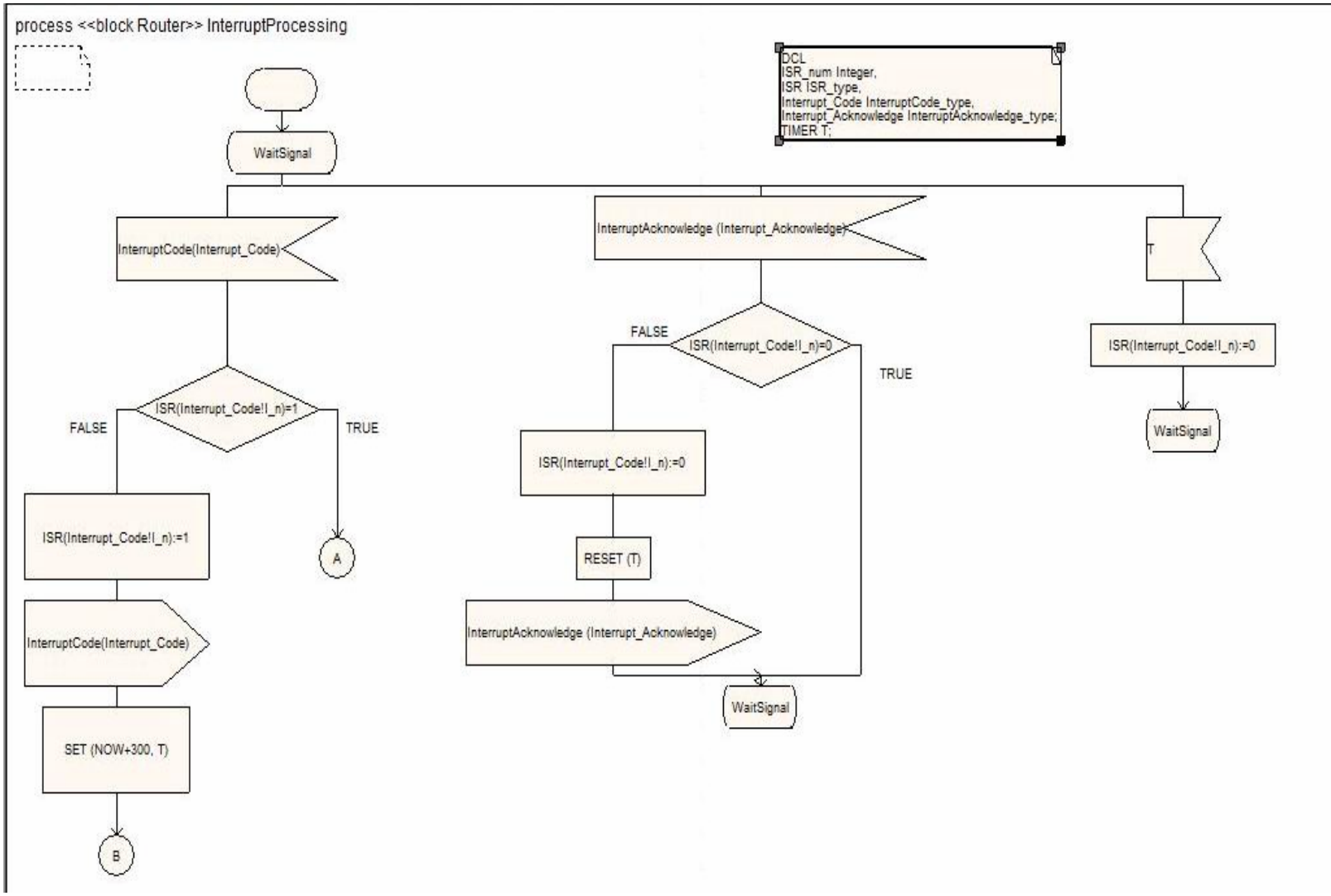
Router:



General description of the Node



General description of the Router

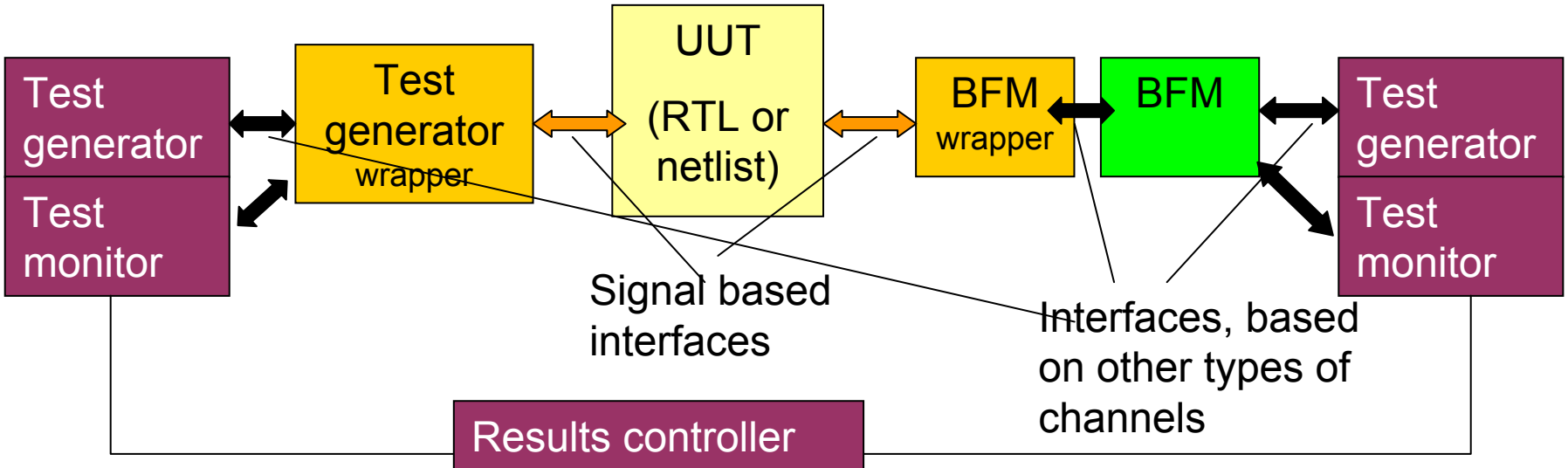


SDL ToolSuite abilities

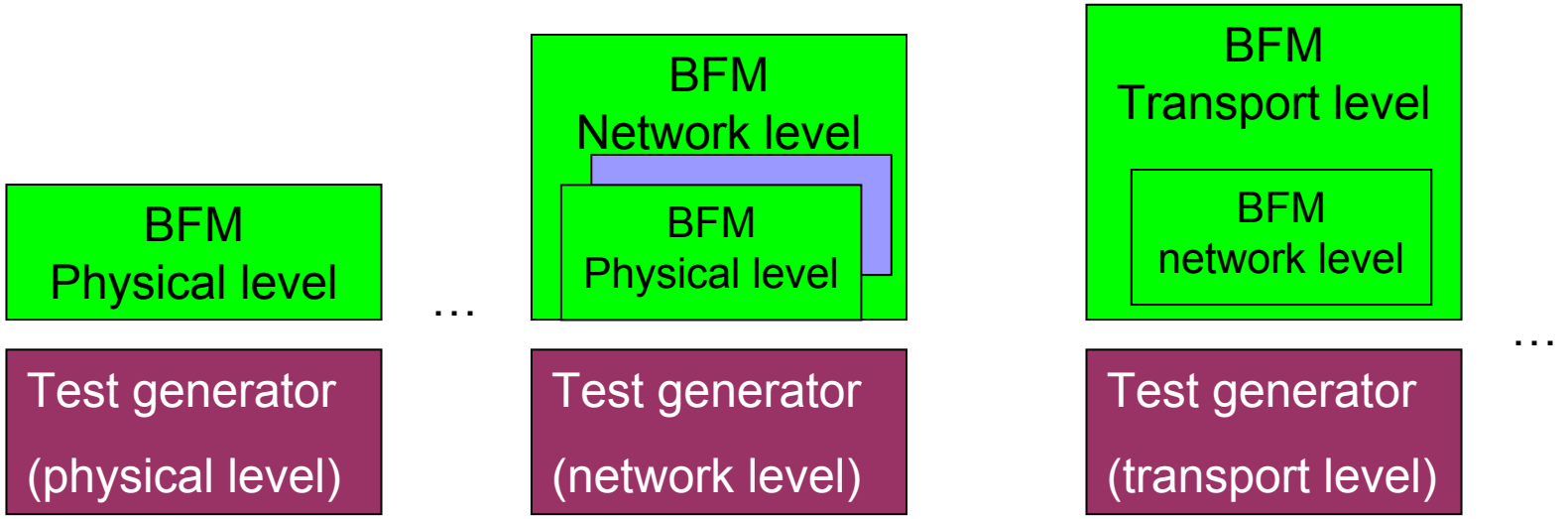
- Realization of specifications (operation simulation)
- Debugging
- Generation of C code
- Validation and verification of the system

Package for test:

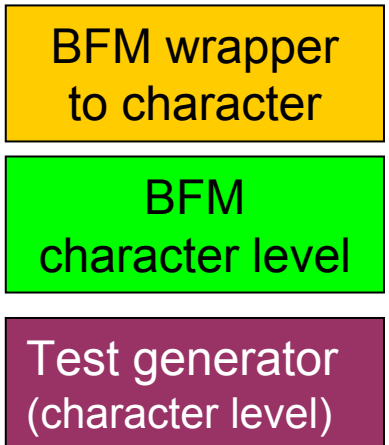
- BFM (base formal model) of protocol stack
- Test generator, test monitor and results controller
- BFM wrapper (for organization of connection between BFM and RTL or netlist)
- Test generator wrapper (for organization of connection between test generator and RTL or netlist)



An hierarchical set of BFMs (example):



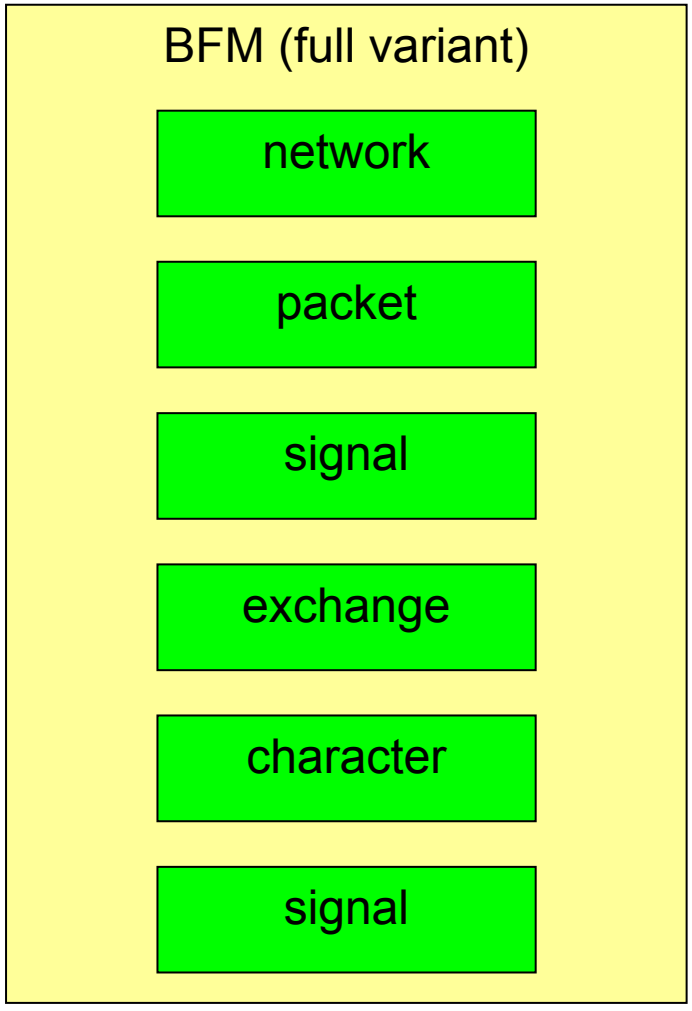
Special generator corresponds to every level of BFM



Often a BFM of one level (or for subgroup of levels, started not from physical) developed

In this case wrapper to correspondent level is developed

Structure of BFM for SpaceWire



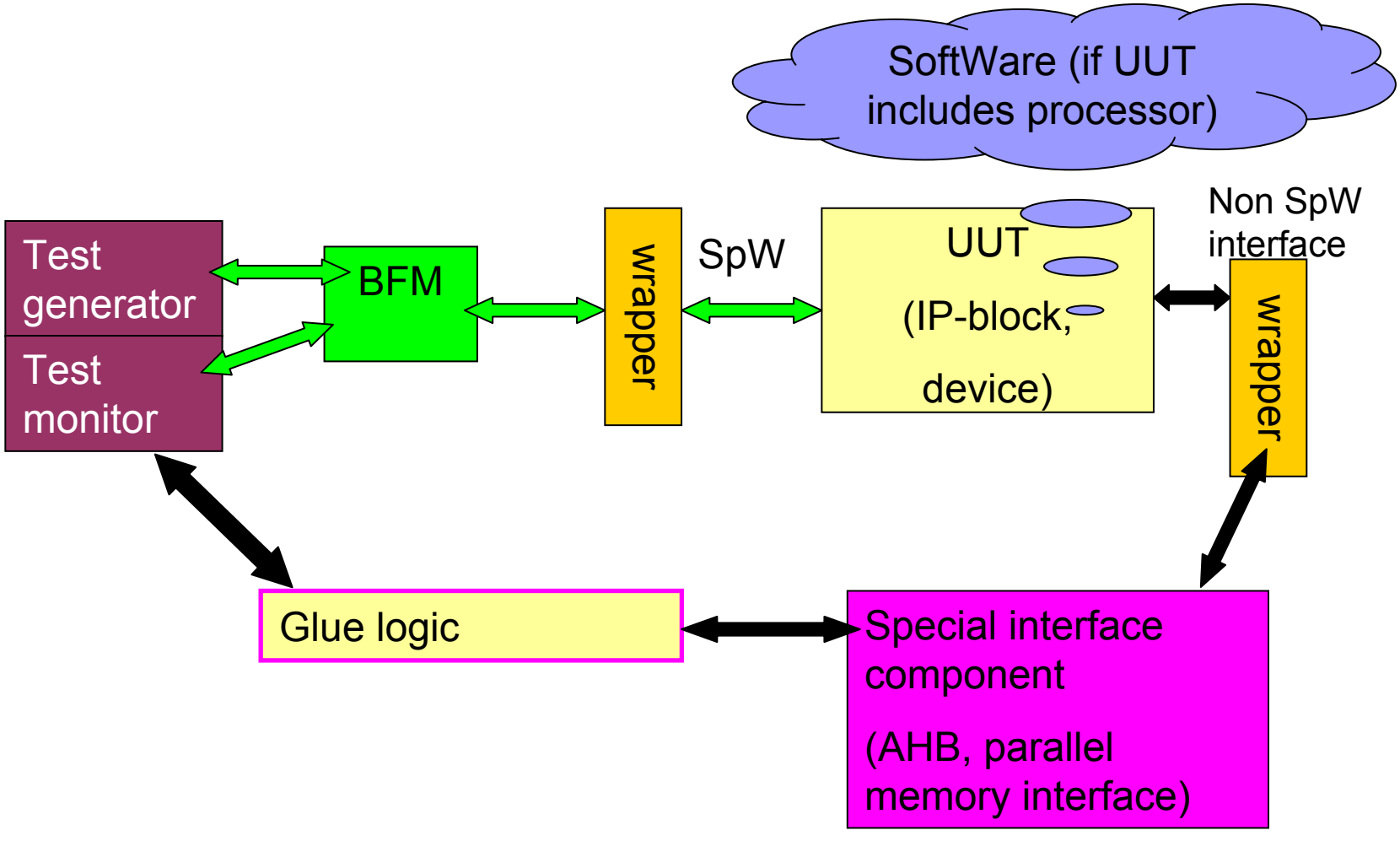
For every subcomponent - test generator

For every subcomponent - wrapper for connection to RTL model or netlist

Every subcomponent includes error generation (translation) mechanism

Additional components for system parameters evaluation

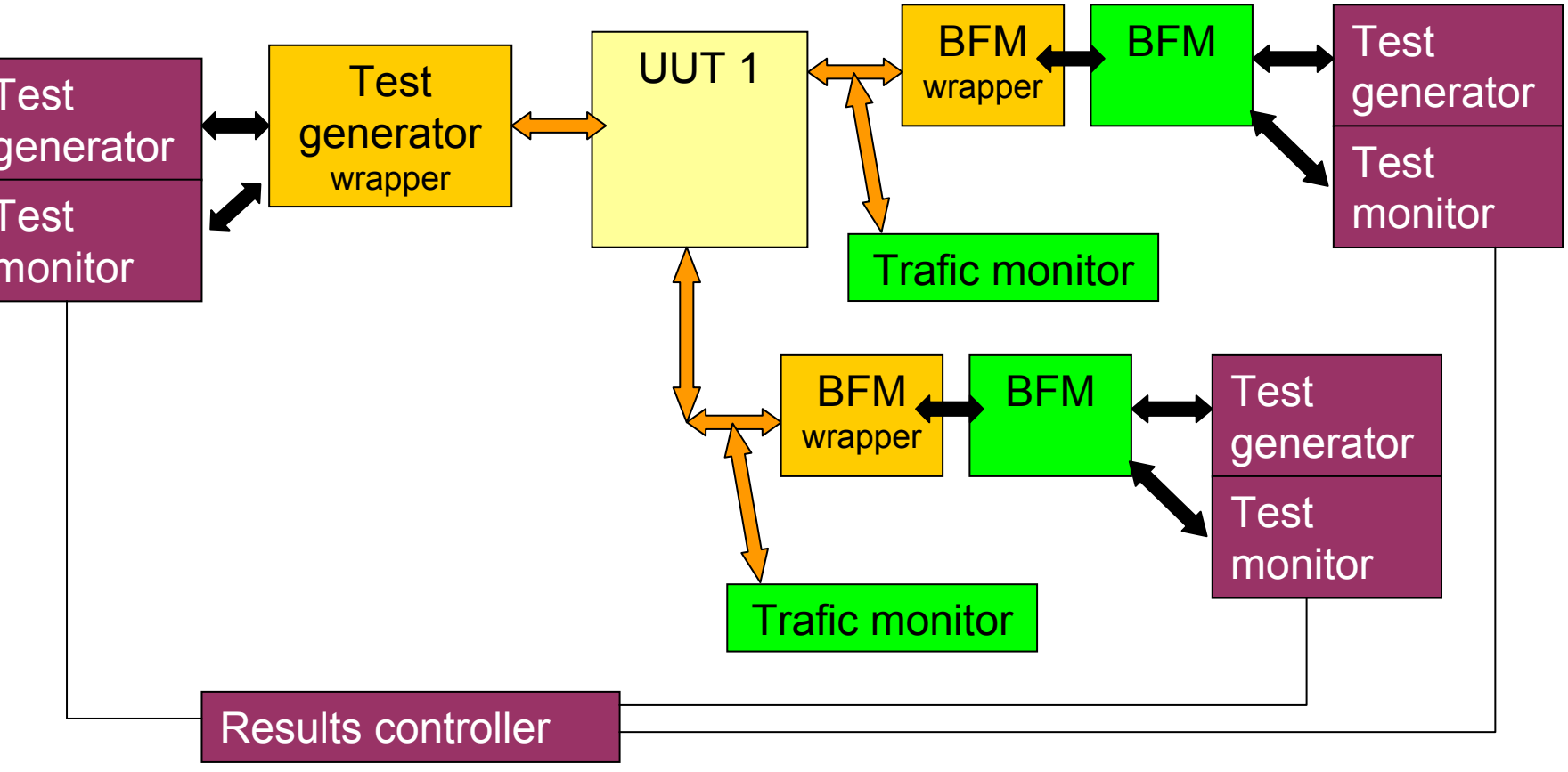
- Traffic monitors
  (for performance evaluation and for error localization)
- Simple switch models
  (for verification of interaction between UUT and a switch)
- Simple memory models
  (for system verification, performance evaluation)


SoftWare (if UUT includes processor)
Test generator
Test monitor
BFM
wrapper
SpW
UUT
(IP-block, device)
Non SpW interface
wrapper
Glue logic
Special interface component
(AHB, parallel memory interface)

Configuration problem:

- IP-block or device should be configured correspondingly test set (for every test)
- In some cases it could be configured via SpaceWire channel, in some cases only via special interface
- Special block to connect test shell to some typical interfaces

Testing and performance evaluation of an UUT with several SpW interfaces



Conclusions

- SDL specifications and BFM set development is reasonable to include in the SpaceWire WG activities
- We shall provide SDL specifications for all our proposals for the next SpaceWire release updates
- SDL specifications and BFM set development is a good subject for distributed developments by SpaceWire WG members
- It can be a good subject for an international project, e.g. under the 7th FW programme.

Thank you