SpaceWire Link interface: LVDS, Power & Cross-strapping Aspects

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AGENDA

- Introduction
- LVDS Technology Overview
- SpaceWire Link Interface & LVDS
- Electrical Understanding of SpW-LVDS Drivers
- Electrical Implementation of LVDS Drivers
  - Dedicated Devices
  - Inside Application Devices
- Recommendation for Electrical Implementation of SpW-LVDS
- Cross-Strapping Requirements
- Failure Propagation Due to Over-Voltage Emission
- Failure Propagation Due to erroneous X-Trapping
- Conclusion

On-board digital systems and logic are becoming more prevalent during the last decade. As a result nowadays, the problem of specifying and designing digital systems for avionics can be considered generally as being successful. (but not always!!!).

A number of recurring problems have been experienced during the different phases: specification, design, development, and testing of System

Not handled correctly at the right time, systems:

- ✓ might become very costly,
- ✓ might require major redesigns,
- ✓ might cause significant schedule delays,
- ✓ or might be launched with a needlessly high level of risk.

Most difficulties have resulted from:

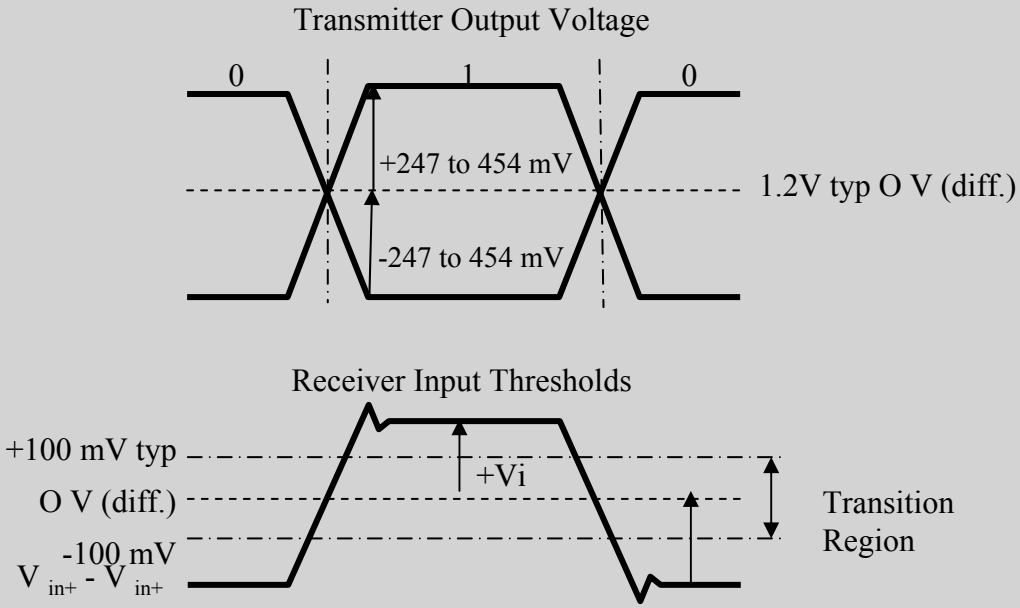
- ✓ Poor design/analysis practices
- ✓ Incomplete knowledge of the newer technologies and related tools coupled with their impact on inherited designs and practices.

LVDS & SpaceWire Link interface & LVDS:
Failsafe Operation, Power & Cross-strapping

LVDS is an Attractive solution which provides

small-swing differential signal for fast data transfers at significantly reduced power

excellent noise immunity versus single-ended transmission standard



In the past LVDS was mostly used for chip-to-chip communication based on CMOS and ECL technologies, then along the time it became more a pervasive technology in network communications

Today, LVDS is a workhorse technology.
Extensively used in many applications: Laptop computers, Imaging and Industrial Vision, Test and Measurement, Medical, Automotive…etc

LVDS ! What else? A Nespresso with George Clooney of course!

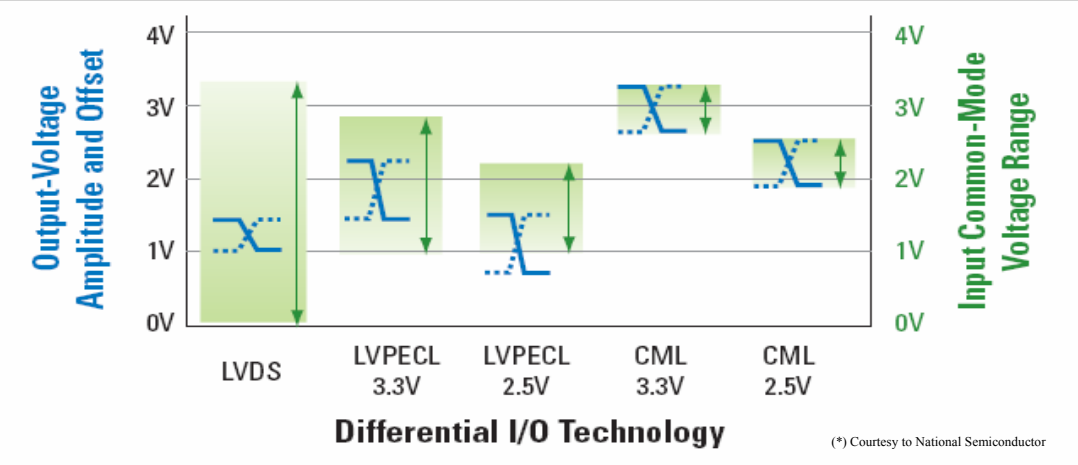
LVDS Industry Standards

LVDS Standard:	Standard Characteristics	Comments
ANSI/TIA/EIA-644-1995:	✓ 3.5mA drive, max data rate of 655 Mbps and theoretical max of 1.923 Gbps based on a loss-less media. ✓ Fail-safe operation of the receiver under fault conditions is discussed ✓ Baseline point-to-point, other configurations issues as multi-receiver operation	✓ ANSI/TIA/EIA-TIA version is the most generic and it is intended to multiple applications
IEEE 1596.3 Scalable Coherent Interface-SCI	✓ is an application specific standard "SCI". Originally electrical specifications were based on ECL technology. ✓ Addresses only high data rate aspects, not low power concerns. Specific encoding for packet switching. ✓ Could be used in single-ended mode over short distances (4 wires)	✓ Features similar: driver output levels, receivers threshold and data rate ✓ Differs in load conditions
ANSI/TIA/EIA-899 – M-LVDS	✓ 10mA drive, ✓ extends from point-to-point applications to multi-point and multi-drop applications ✓ M-LVDS (& B-LVDS) products are capable of data rates in excess of 3 Gbps.	✓ B-LVDS features only similar voltage swing
G-LVDS proprietary standard	✓ Does not specify any transmitter drive current ✓ Places the driver output voltage offset closer to ground potential.. ✓ Point-to-point	✓ G-LVDS is widely used in Telecom industry

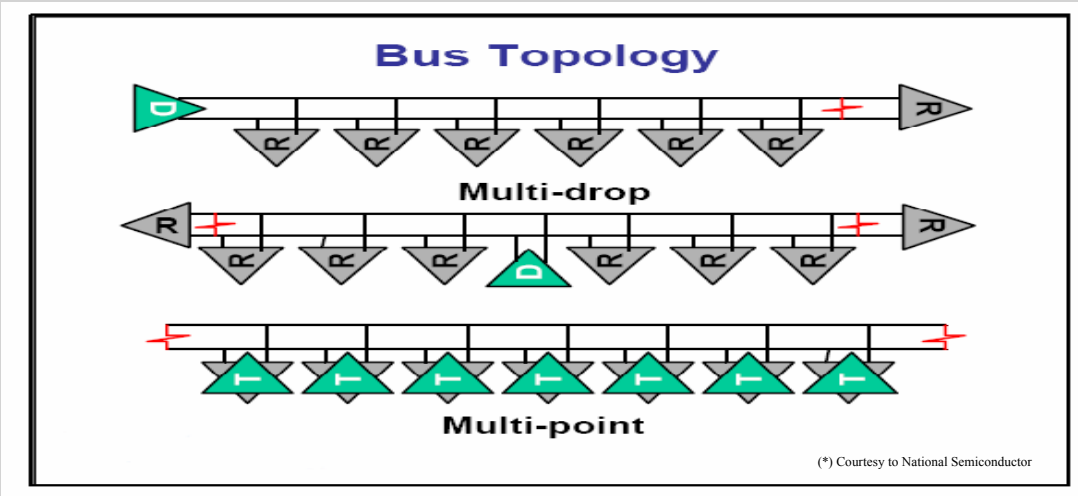
Parameter	LVDS	BLVDS	M-LVDS	GLVDS
TX VOD	250 – 450 mV	240 – 500 mV	480 – 650 mV	150 - 500 mV
TX VOS	1.125 V	1.3 V	0.3 – 2.1 V	75 – 250 mV
TX RL	100 Ω	27 - 50 Ω	50 Ω	Internal to RX
TX IOD	2.5 – 4.5 mA	9 – 17 mA	9 – 13 mA	adjustable
TX IOS	<24 mA	< 65 mA	< 43 mA	-
RX VTH	+/-100 mV	+/-100 mV	+/-50 mV	+/-100 mV
RX Vin	0 to +2.4 V	0 to +2.4 V	-1 to 3.8 V	-0.5 to 1 V
VCM	+/-1 V	+/-1 V	+/-2 V	+/-0.5 V

LVDS Implementation and Usage

1 - LVDS implemented on different technologies

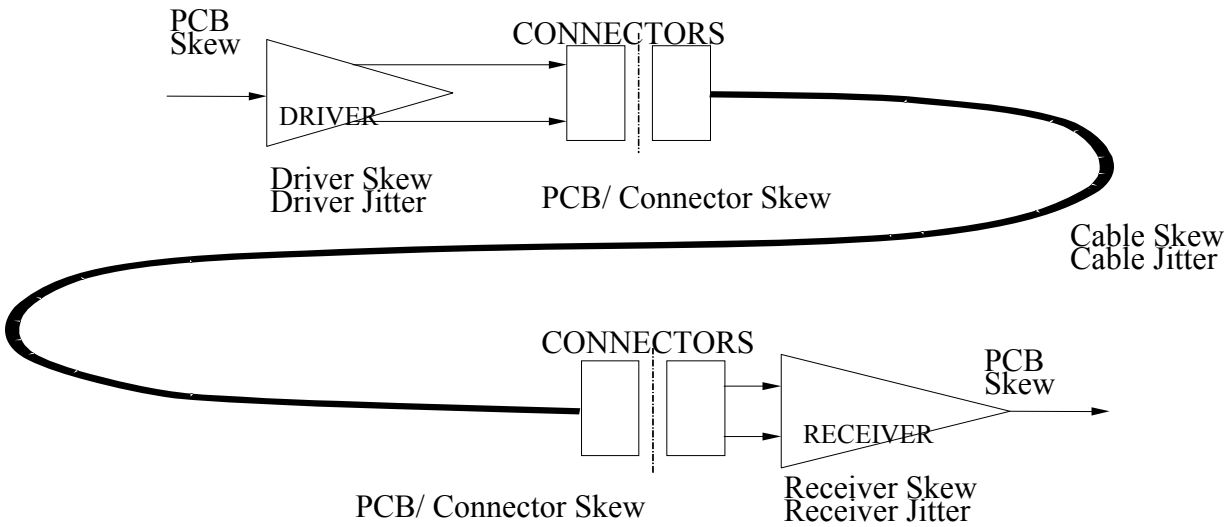


2 -LVDS implemented for different bus topologies

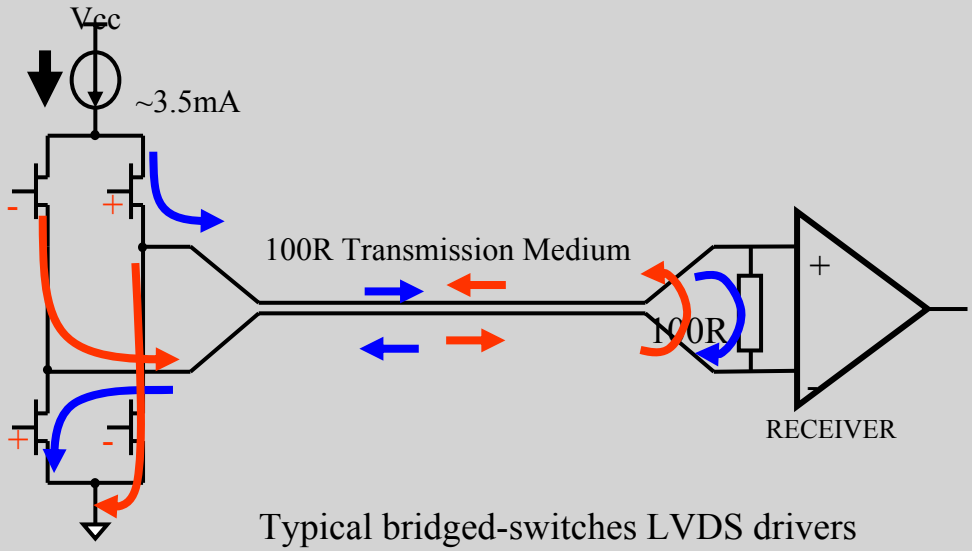


SpaceWire Link Interface (ECSS-E50-12A): full-duplex, point-to-point, serial data communication links based on:

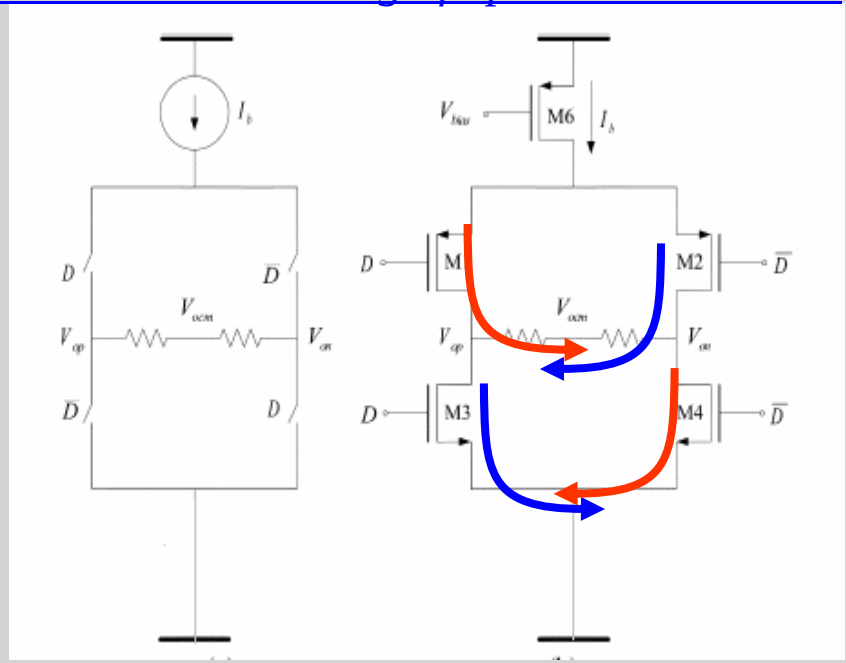
- Cables ESCC detail specification No 3902/003
- Connectors: ESCC detail specification No 3401/071
- LVDS drivers**: ANSI/TIA/EIA-644**



Designs and/or Implementations of SpW-Link-I/Fs for SpaceWire Network based on Bus-Topology and related LVDS (i.e BLVDS, MLDS, GLVDS…etc) are considered as non-compliance to the ECSS-E50-12A.



Typical bridged-switches LVDS drivers



Simple functioning:

if switches M1 & M4 are on (switches M2 & M3 are off) ⇒ the polarity of the output current and voltage is positive. .

if switches M1 & M4 are off (switches M2 & M3 are on) ⇒ the polarity of the output current and voltage is reversed.

Summary of ANSI/TIA/EIA-644

Specification	ANSI/TIA/EIA-644 Min	ANSI/TIA/EIA-644 Max	Typ
Output Current	2.47 mA	4.54 mA	Determined by RSET (nominally 3.5 mA)
Differential Output Voltage Magnitude	247 mV	454 mV	350 mV
Output Offset Voltage (Common Mode)	1.125 V	1.375 V	1.2 V
Transition Time: Rise Time (t_R) and Fall Time (t_F); 20% to 80%		$\leq 0.3 \times t_{UI} = 0.3 \times 5.88$ ns = 1.76 ns	0.5 ns

ECSS-E50-12A/Section 4.3.2: ~ 3.5mA constant current to produce output signal swing of 350 mV, .CMV at least ± 1v

LVDS implementation Options:

- Outside Application Devices (Vendors as AeroFlex, NS, TI…..)
- Inside Application Devices: Inside FPGA or Inside ASIC

1. Outside Application Devices

Example: **Aeroflex** set of quad drivers and quad receivers - 5V power supply or 3.3V power supply

FEATURES

- >155.5 Mbps (77.7 MHz) switching rates
- ±340mV nominal differential signaling
- 5 V power supply
- TTL compatible inputs
- Ultra low power CMOS technology
- 5.0ns maximum, propagation delay
- 3.0ns maximum, differential skew
- Radiation-hardened design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 300 krad(Si) and 1Mrad(Si)
  - Latchup immune (LET > 100 MeV-cm^2/mg)
- Packaging options:
  - 16-lead flatpack (dual in-line)
- Standard Microcircuit Drawing 5962-95833
  - QML Q and V compliant part
- Compatible with IEEE 1596.3SCI LVDS
- Compatible with ANSI/TIA/EIA 644-1996 LVDS Standard

ABSOLUTE MAXIMUM RATINGS[1]
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 6.0V
V_{IO}	Voltage on any pin	-0.3 to (V_{DD} + 0.3V)
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.25 W
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	10°C/W
I_I	DC input current	±10mA

FEATURES

- >400.0 Mbps (200 MHz) switching rates
- ±340mV nominal differential signaling
- 3.3 V power supply
- TTL compatible inputs
- Cold sparing all pins
- Ultra low power CMOS technology
- 1.5ns maximum, propagation delay
- 310ps maximum, differential skew
- Radiation-hardened design; total dose irradiation testing t MIL-STD-883 Method 1019
  - Total-dose: 300 krad(Si) and 1Mrad(Si)
  - Latchup immune (LET > 100 MeV-cm^2/mg)
- Packaging options:
  - 16-lead flatpack (dual in-line)
- Standard Microcircuit Drawing 5962-98651
  - QML Q and V compliant part

ABSOLUTE MAXIMUM RATINGS[1]
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 4.0V
V_{IO}	Voltage on any pin during operation	-0.3 to (V_{DD} + 0.3V)
	Voltage on any pin during cold spare	-.3 to 4.0V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.25 W
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	10°C/W
I_I	DC input current	±10mA

Recommendation for SpW-Link-I/F:
Use SpW transmitters and receivers with same bandwidth.

Recommendation for SpW-Link-I/F:
Use SpW drivers/receivers with same V_{DD}

Problem for LVDS: drivers have a vis-à-vis device electrically connected but without power supply. (http://www.national.com/an/AN/AN-1194.pdf)
Trick is cold sparing capabilities: the spare must present a high-input impedance to the system without drawing power.

Recommendation for SpW-Link-I/F:
Use SpW drivers with cold sparing capabilities

2. Inside Application Devices

Example 1: – SpW-Router is the heart of the SpW Network

SpW_10X (AT910E) (Atmel MH1RT Rad Hard 0.35 µ m CMOS library providing Cold Sparing I/O Buffers

WARNING

Since LVDS is based on a current loop it should not matter what the supply voltage is to an LVDS device connected to the SpW-10X router. However, there is a potential problem when connecting to devices with power supplies greater than 3.3 V, which is the supply voltage of the SpW-10X device. It should be emphasised that during normal operation there is no problem, but if the LVDS device connected to the SpW-10X device can fail in such a way as to put a higher voltage than 3.3 V on to the pins of the SpW-10X device then this can cause a problem. The simplest way to overcome this potential problem is to ensure that the LVDS devices driving the SpW-10X device are all powered by 3.3V.

Recommendation: Use the same power supply for SpW transmitters and related receivers in SpW Network

Example 2: Actel FPGA (http://www.actel.com/documents/ax_lvds_an.pdf)

LVDS/Inputs and Receivers

Axcelerator LVDS receivers, **which are not current-mode receivers**, conform to all the electrical specifications defined in the ANSI/TIA/EIA-644 specification. This is none sense since all the receiver are voltage receivers

LVDS/Output and Transmitters

Axcelerator and RTAX-S/SL devices **do not have embedded current-mode LVDS transmitters** in the I/O cells. Instead, LVDS data is transmitted on two single-ended I/Os through an external resistor termination network that reproduces the required LVDS differential current and voltage.

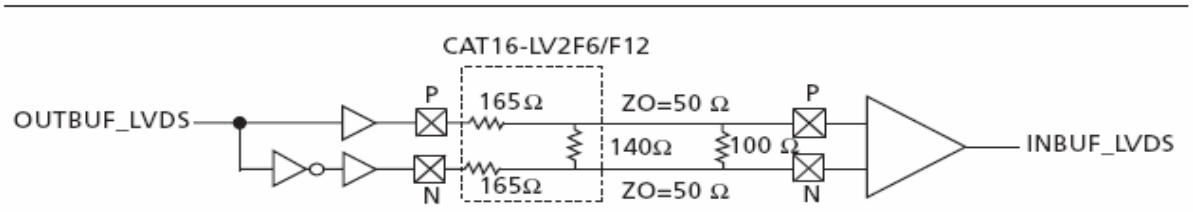


Figure 9 • **LVDS Point-to-Point Circuit in Axcelerator**

Axcelerator and RTAX-S/SL LVDS are considered as non-compliance to the ECSS-E50-12A.

Recommendation
Use outside devices for SpW drivers and receivers with Actel FPGAs.

	Strong Recommendations	Remarks
LVDS Std	ANSI/TIA/EIA-644	No any other industrial or proprietary standard
Serial Communication Type	Point-to-Point	No Multi-point, No Multidrop (B-LVDS, M-LVDS
Technology	CMOS Technology with enough headroom (> 2V),	Issue for future CMOS technologies (example: CMOS technology ranging from 0.25 µm channel length at 2.5 V down to sub-0.1 µm at 1 V)
Driver Type	Unlike CMOS, which is typically a voltage output, LVDS is a current output technology ⇒ Courant source driver	No voltage source
Power Supply	Same power supply range for SpW driver and SpW receiver	If you use ESA ASSP(s) as SpW-X10 and SpW_RTC, V_{DD} (0.3V to 4.0V)
Bandwidth	Same bandwidth range for SpW driver and SpW receiver	If you use ESA ASSP(s) as SpW-X10 and SpW_RTC ~ 200 Mbps
Failsafe Operation	Cold sparing capabilities to handle failsafe operation	Cold sparing capabilities handle cold redundant system without power supply

SIGNAL X-COUPLING

THE SYSTEM ENGINEER'S BLESSING

THE POWER ENGINEER'S NIGHTMARE

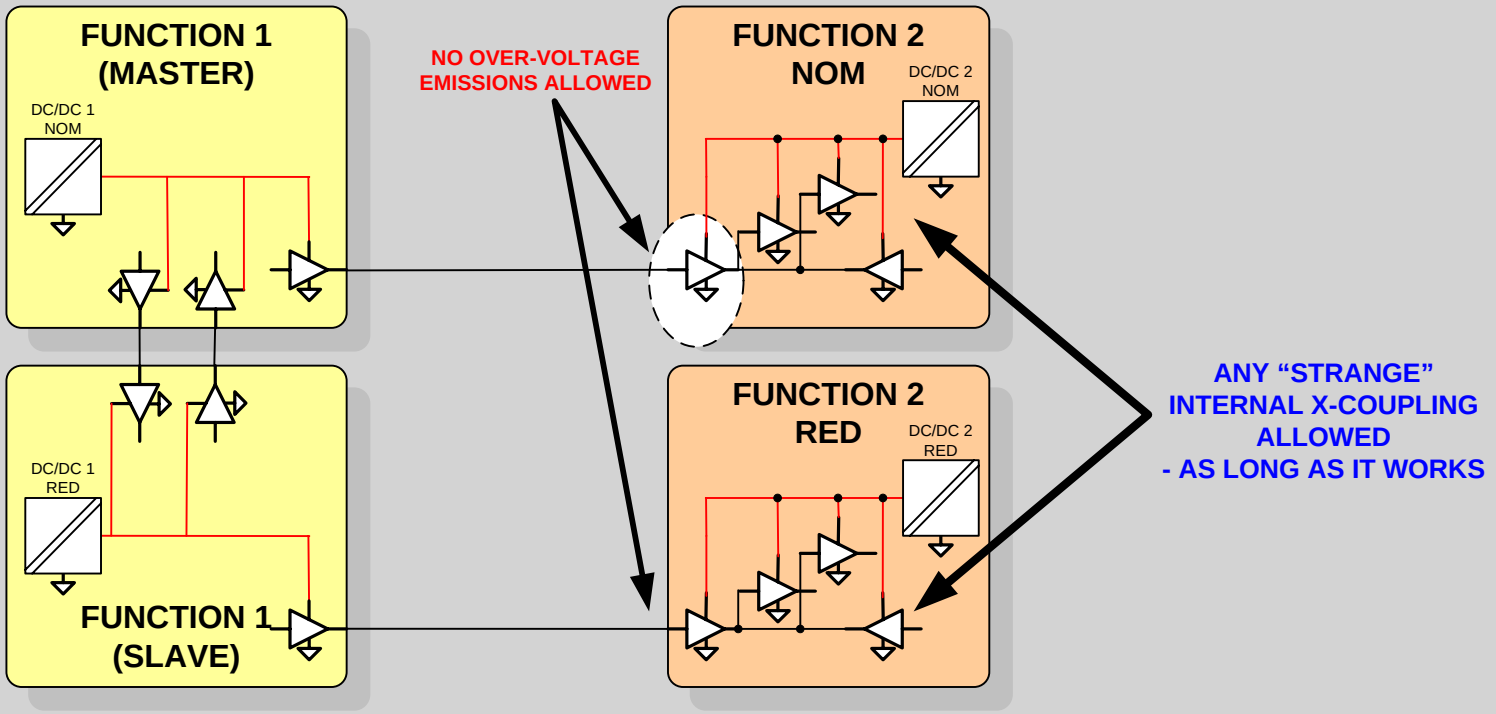
SOME IMPORTANT TOPICS TO LOOK IN TO

1. "X-STRAPPING" IN REDUNDANT SYSTEMS -> REQUIREMENTS
2. FAILURE PROPAGATIONS DUE TO ERRONEOUS X-COUPLING
3. FAILURE PROPAGATION DUE TO OVERVOLTAGE EMISSION
4. BACK-POWERING IN COLD REDUNDANCY
5. IMPORTANCE OF DECOUPLING AND POWER QUALITY FOR LVDS
6. CLASSICAL X-COUPLING DESIGN FLAWS
7. POWER DISSIPATION ASPECTS

We are usually implementing X-coupled interfaces in three ways

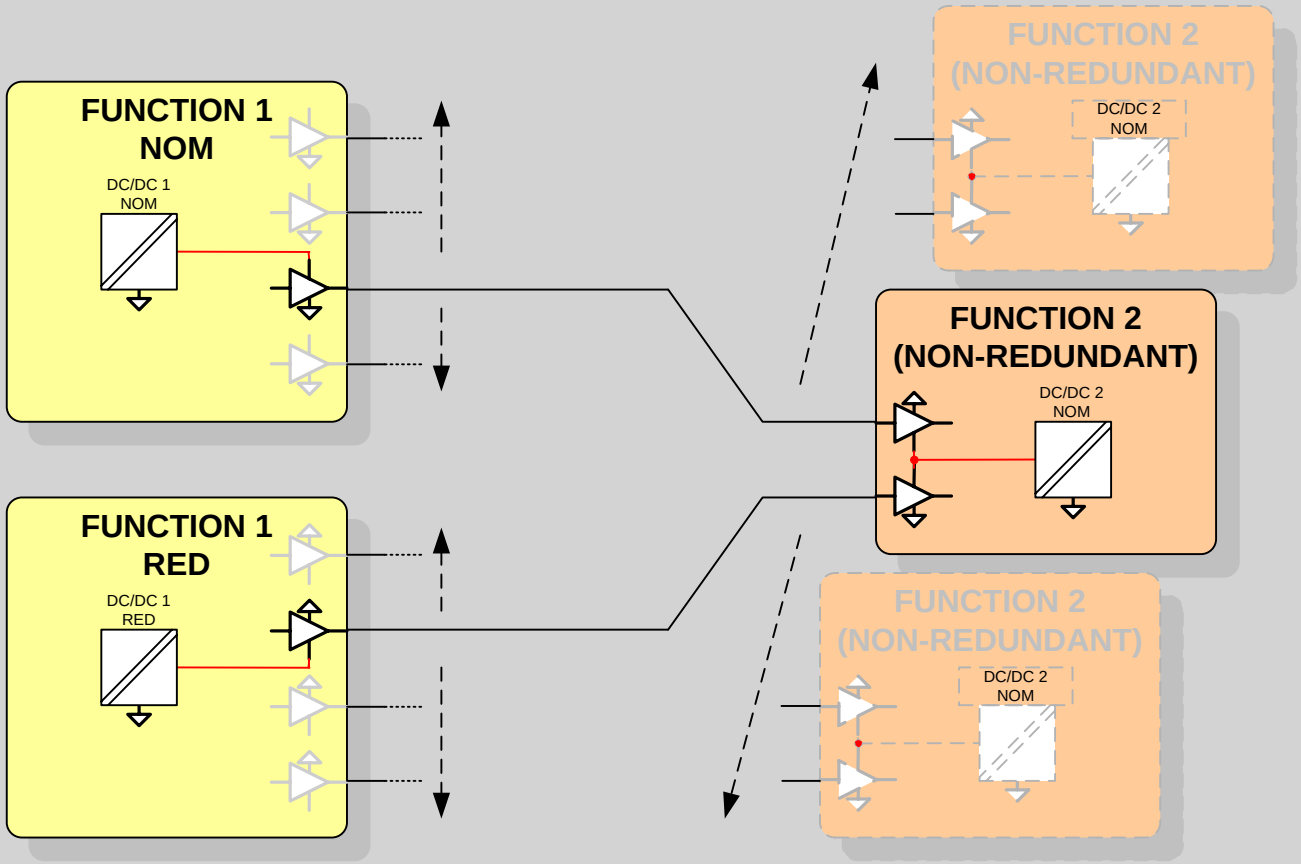
1. X-coupling within the same "functional group", which usually means within one PCB or within one out of two redundant units.

   - One component failure is allowed to disable the unit function, but not to impose any stress (as over-voltage) to any other unit



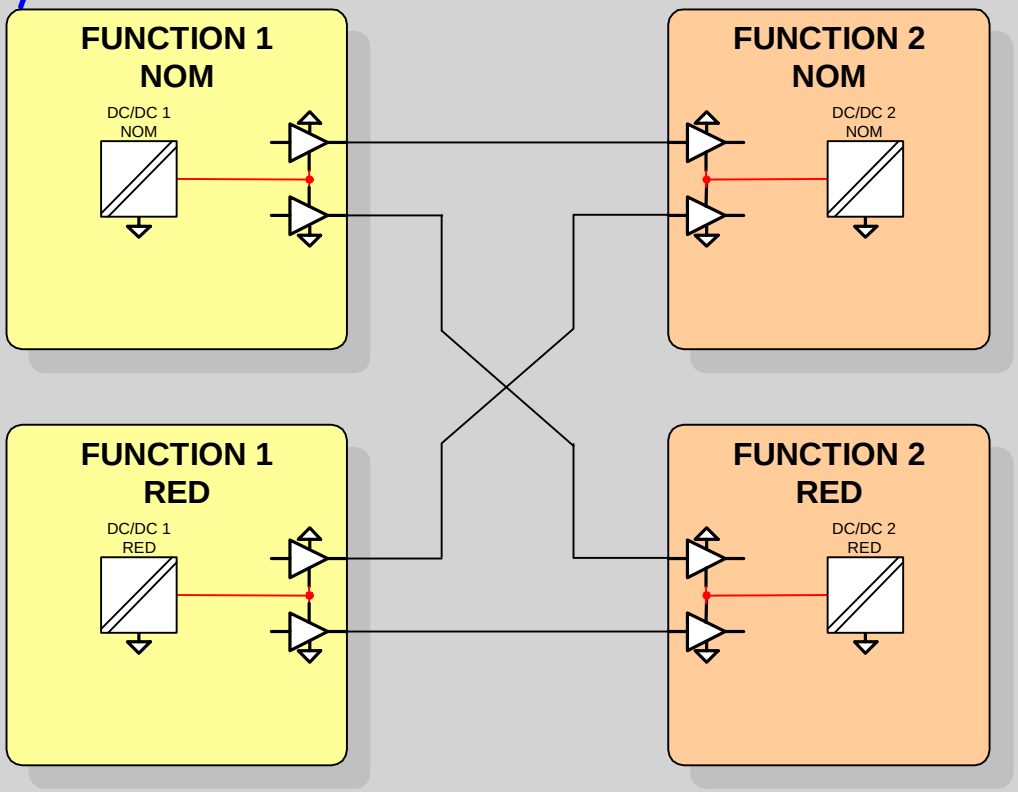
2. X-coupling between 2 redundant units and 1 non-redundant unit

- One I/F component failure on function 1 shall not propagate a permanent failure to the redundant unit, nor to non-redundant unit

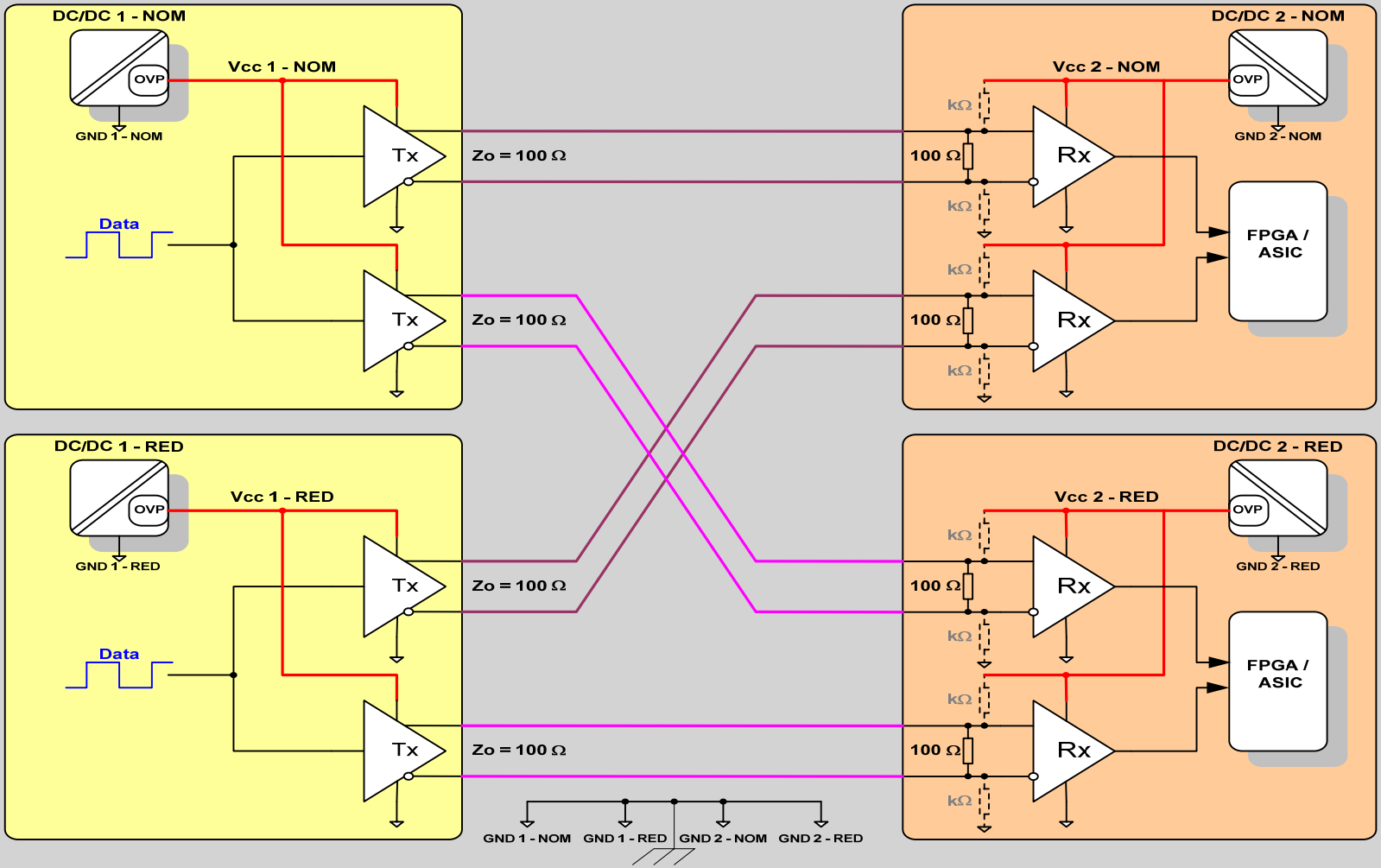


3. Full X-coupling of two Units Nom and Red units (2 functionalities).

- One I/F component failure shall not cause permanent failure propagation to the redundant unit of the same functionality
- One I/F component failure shall not cause permanent failure propagation to any of the interfacing units of the other functionality.



THE "FULL X-COUPLING" OF A DIFFERENTIAL INTERFACE "POINT - TO - POINT"

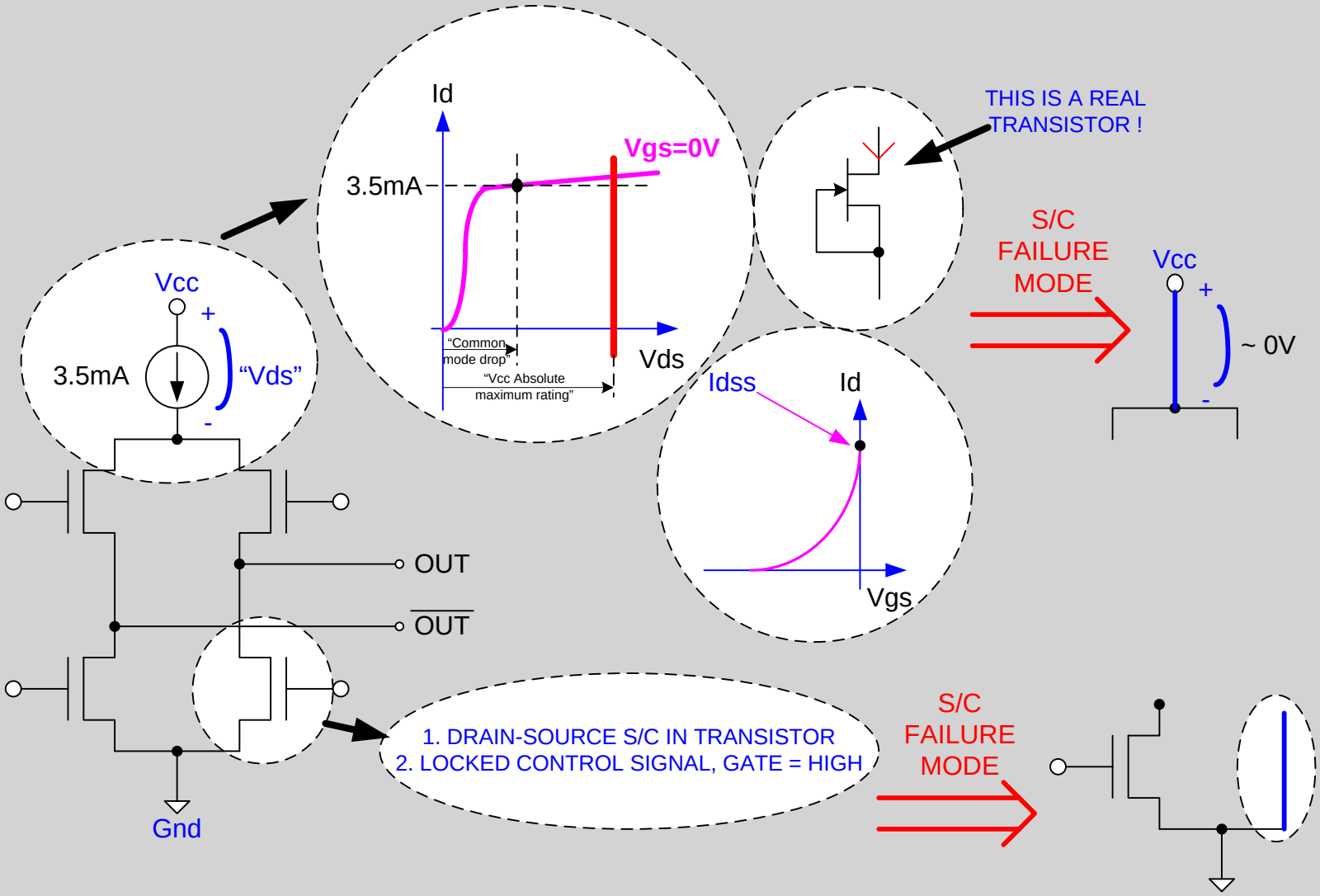


- NO OTHER WAY OF FULL X-COUPLING IS WANTED BY ESA !!

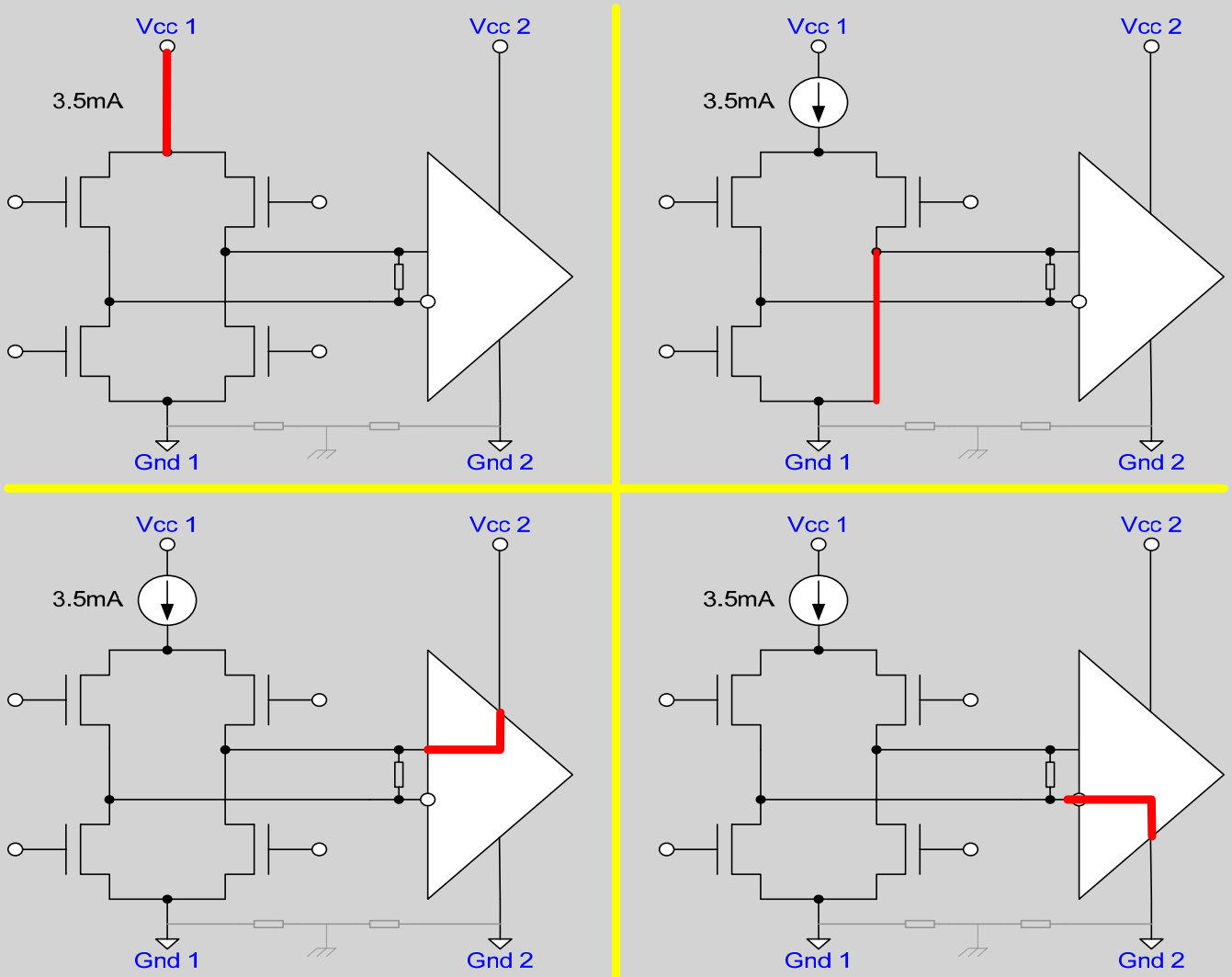
THE GUIDE TO A ROBUST / RELIABLE SYSTEM

1. A SINGLE TRANSMITTER CIRCUITRY SHALL BE CONNECTED **ONLY** IN "POINT-TO-POINT" TO A SINGLE RECEIVER CIRCUITRY.
2. ALL POWERING OF EXTERNAL (LVDS) I/F CIRCUITRY IN A X-COUPLING, **SHALL** BE OVER-VOLTAGE PROTECTED BELOW THE CIRCUIT'S ABSOLUTE MAXIMUM VCC RATINGS
3. TRANSMITTER AND RECEIVER CIRCUITS SHALL USE THE SAME VCC LEVEL, I.E. IF ONE UNIT HAS +3.3V CIRCUIT – THE RECEIVER SHALL ALSO HAVE +3.3V CIRCUITS.
4. LVDS RECEIVERS SHALL HAVE "SAFETY-PULLUP" ON INPUTS
5. AN LVDS RECEIVER SYSTEM SHALL WORK WITH A TRANSMITTER HAVING AN UNDEFINE IMPEDANCE TO GND AFTER 1 FAILURE
6. ALL LVDS CIRCUITRY SHALL HAVE A GOOD POWER SUPPLY DECOUPLING ON THE VCC NODE

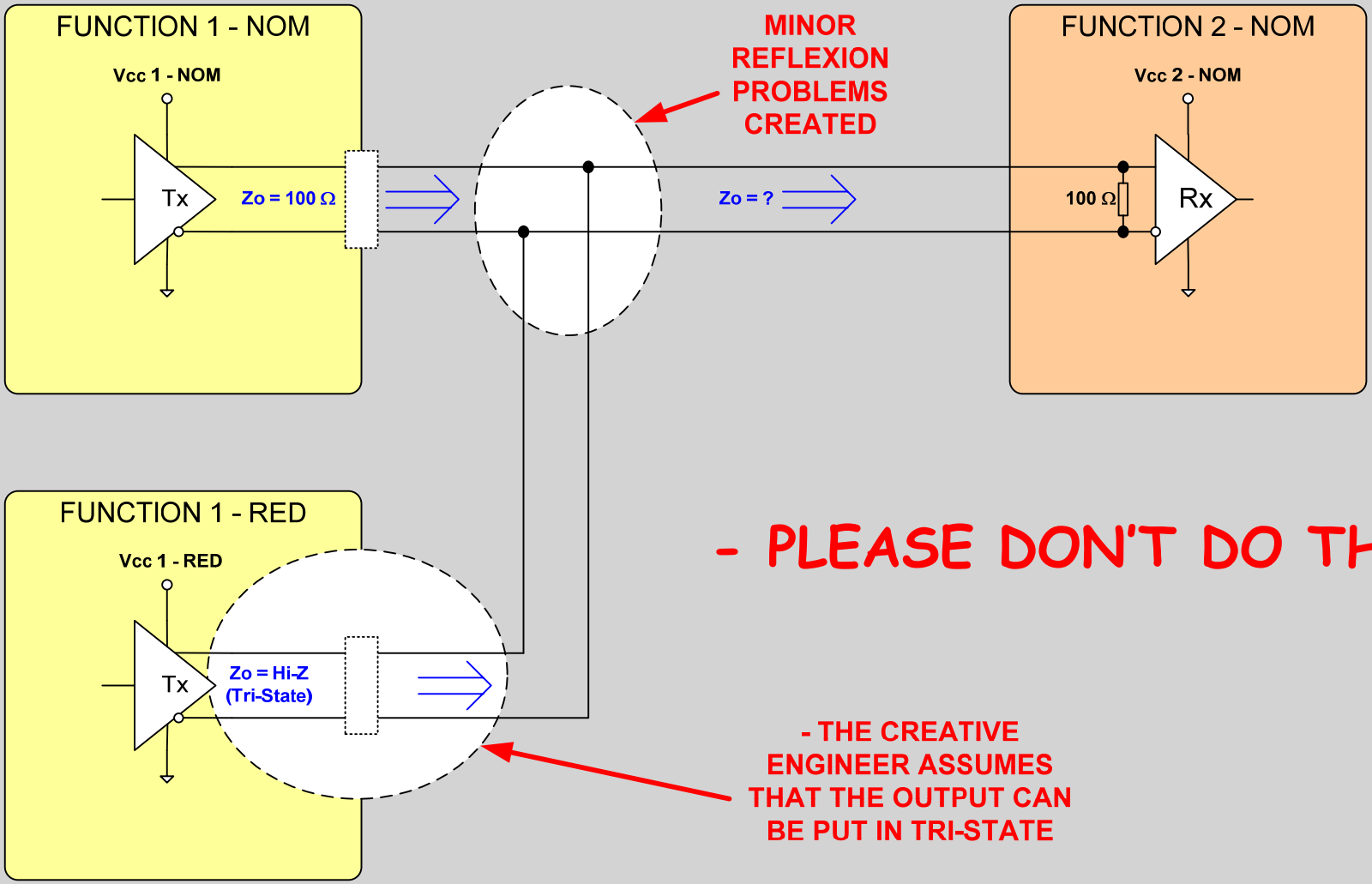
HW FAILURE MODES IN THE LVDS TRANSMITTER



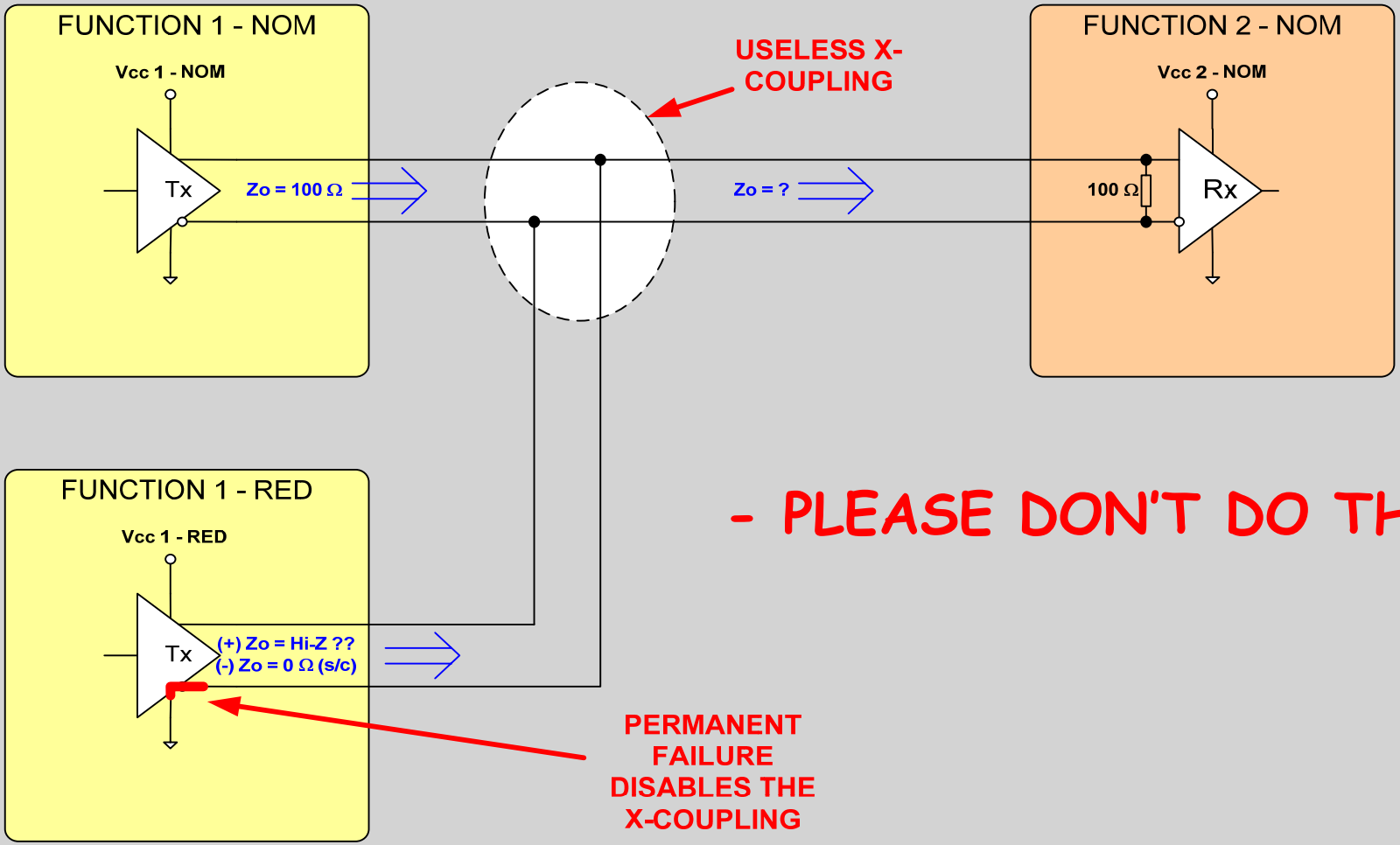
FAILURE MODES IN THE LVDS Tx – Rx SYSTEM



ERRONEOUS X-STRAPPING ON TRANSMITTER SIDE (1)

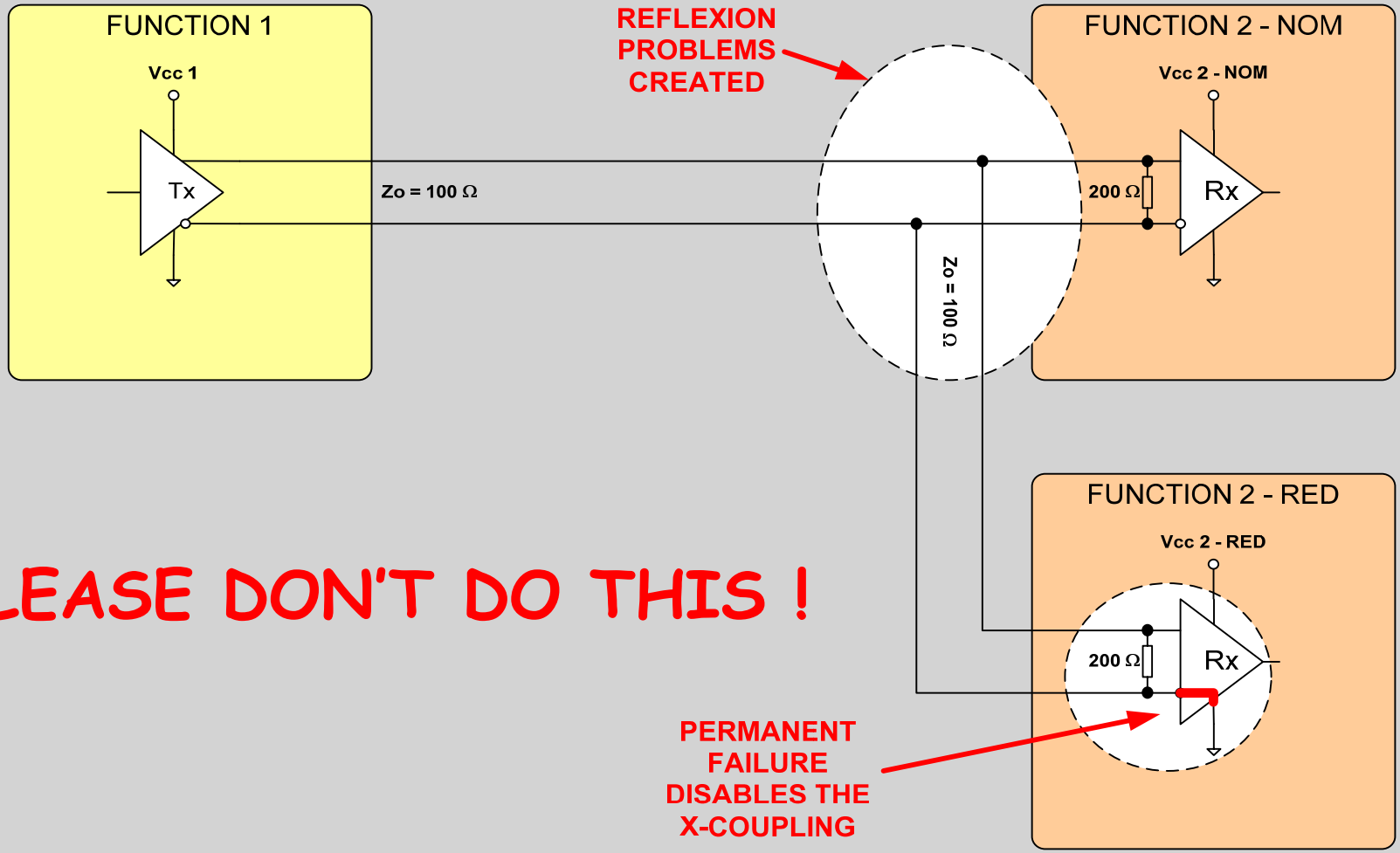


ERRONEOUS X-STRAPPING ON TRANSMITTER SIDE (2)



- PLEASE DON'T DO THIS !

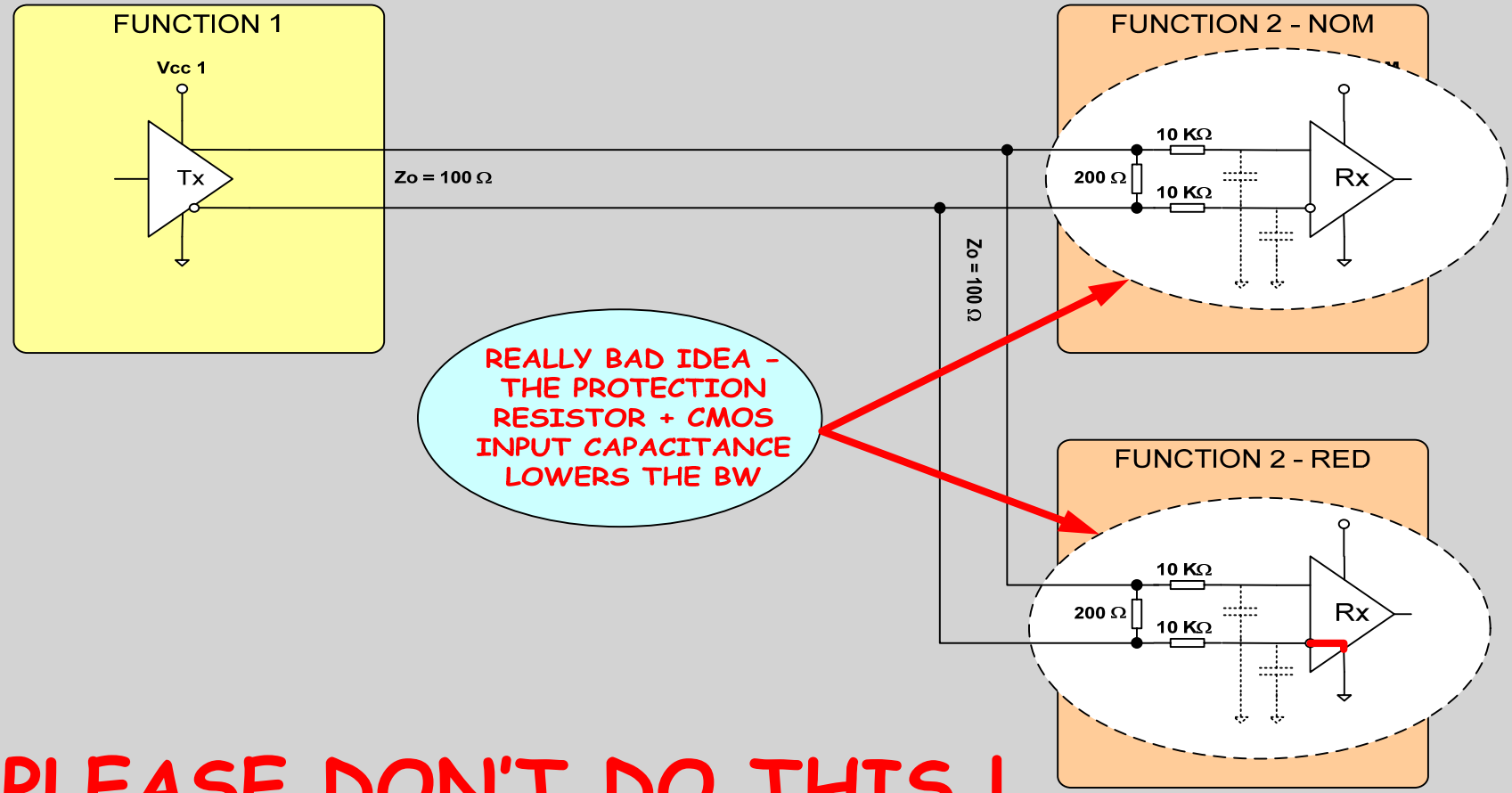
ERRONEOUS X-STRAPPING ON RECEIVER SIDE (1)



- PLEASE DON'T DO THIS !

ERRONEOUS X-STRAPPING ON RECEIVER SIDE (2)

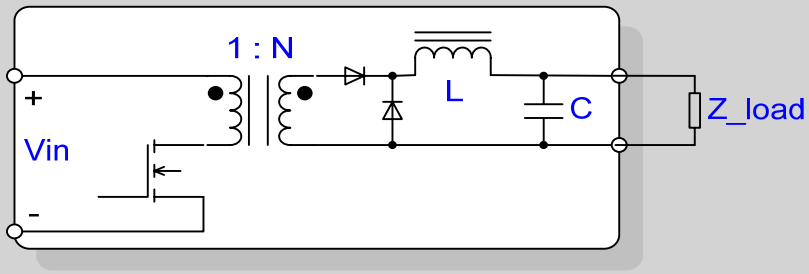
- THE CREATIVE ENGINEER STEPS IN....(WITH A BAD IDEA)

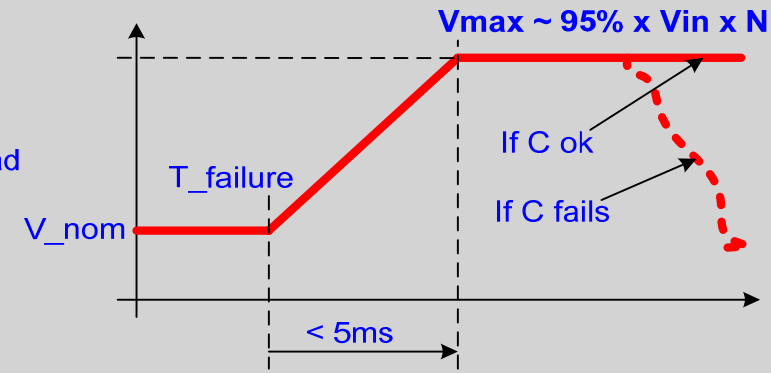


- PLEASE DON'T DO THIS !

HOW DOES A POWER SUPPLY BEHAVE IN FAILURE MODE (CONTROL CIRCUIT FAILURE) AND WITHOUT OVER-VOLTAGE PROTECTION?

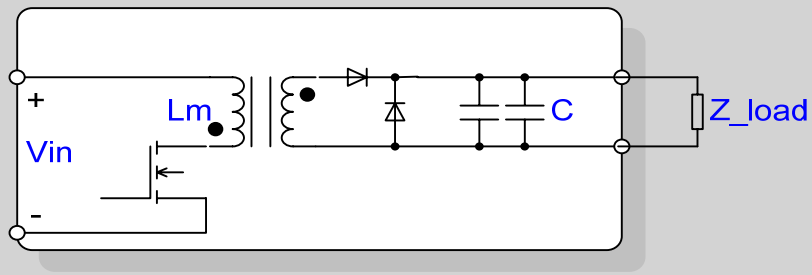
FORWARD TOPOLOGY CONVERTER

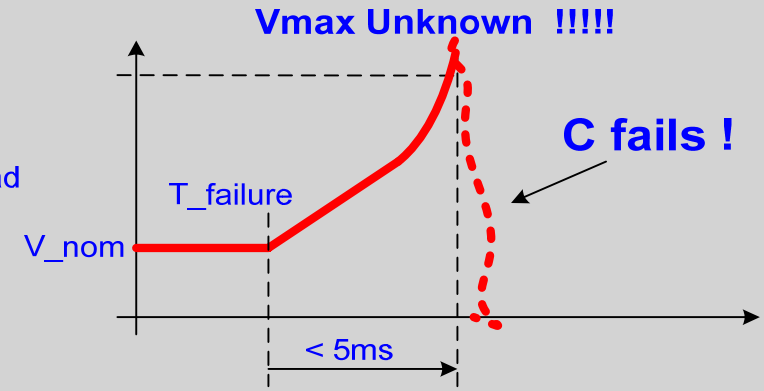




1. Maximum level is predictable, and if C is rated high enough – the over-voltage emission is permanent
2. The rise-time is predictable, but is dependant on all parameters – fsw, L, C, Z_load and Vin

FLYBACK TOPOLOGY CONVERTER





1. Maximum level is **NOT** predictable, and is likely to happen when any output capacitor is failing in S/C
2. The rise-time is somewhat predictable, but is dependant on all parameters – fsw, Lm, C, Z_load and Vin

N-O-T-A B-E-N-E !!!

POINT 1

SO CALLED "OFF-THE-SHELF" DC/DC CONVERTER HYBRIDS –
SOME OF THEM WHO'S NAME IS STARTING WITH THE LETTER "I…" AND SOME OF THEM STARTING WITH THE LETTER "V…"
– ARE VERY OFTEN DESIGNED AS FLYBACK AND DOES

NOT

HAVE OVER-VOLTAGE PROTECTION !!!!!

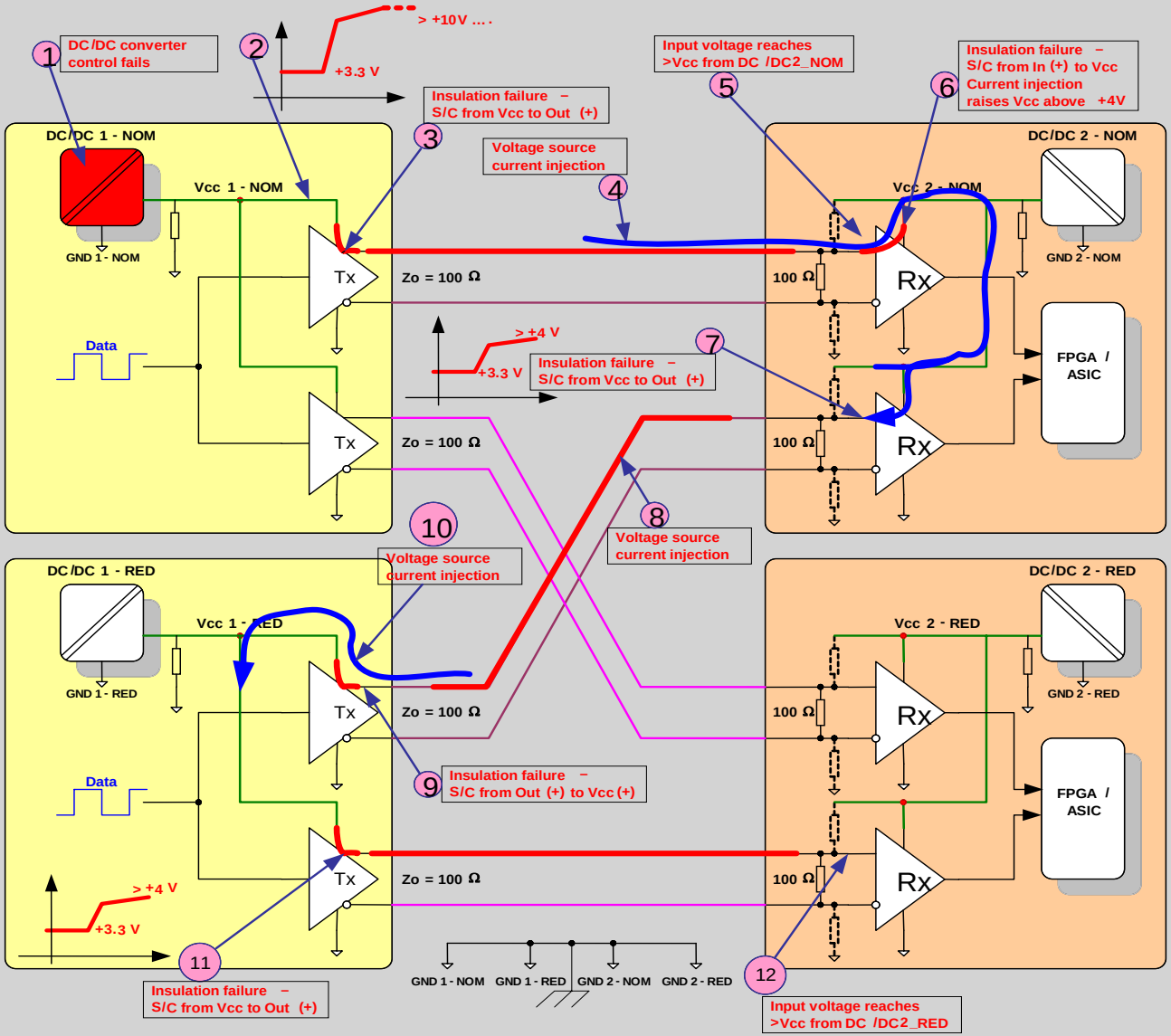
POINT 2

IF THE OVERVOLTAGE MAXIMUM PEAK IS NOT POSSIBLE TO ANALYSE (=FLYBACK), THEN A VOLTAGE CLAMPING LOCALLY ON I/F LEVEL IS

NOT

EASILY ANALYSED TO A SAFE DESIGN.

THE IMPORTANCE OF HAVING OVER-VOLTAGE PROTECTION

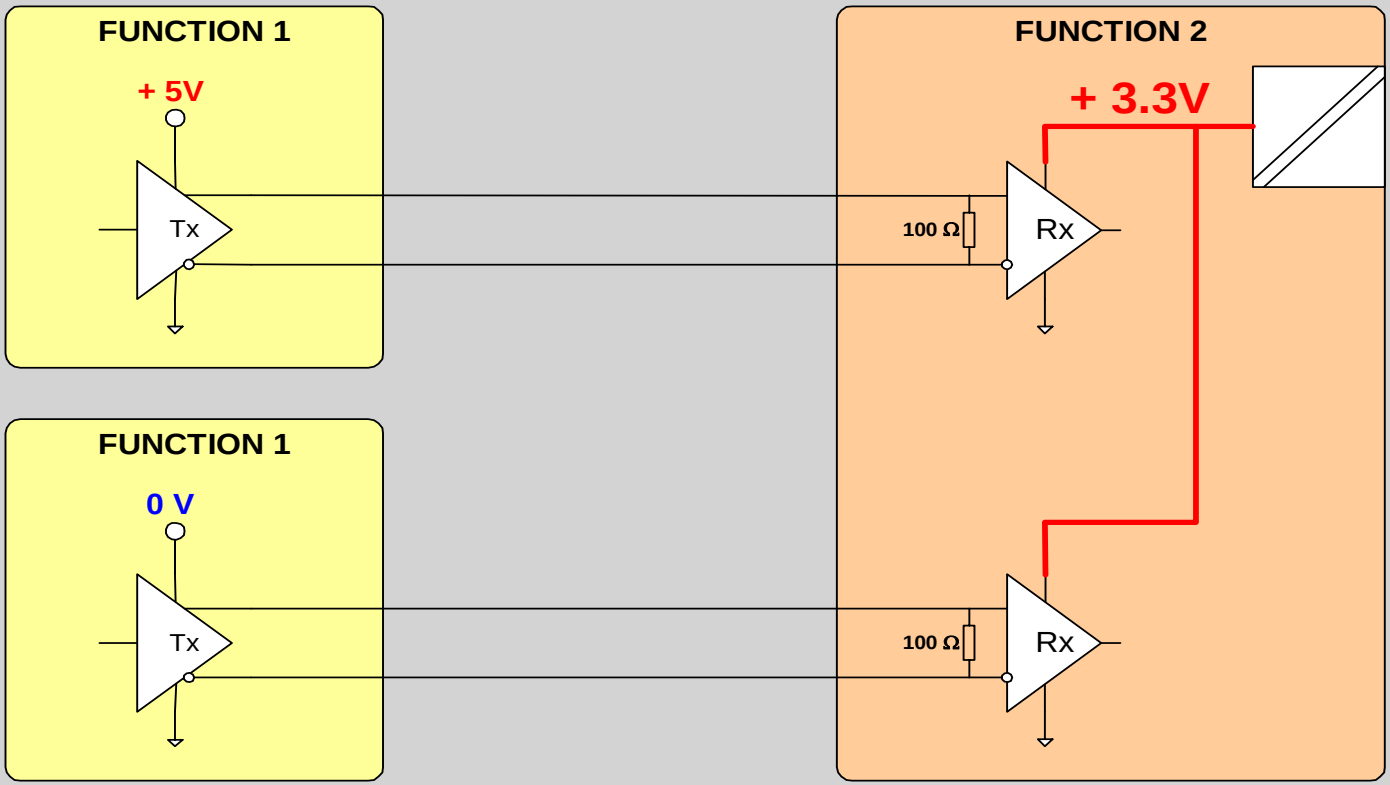


REPETITION OF MANTRA !!!

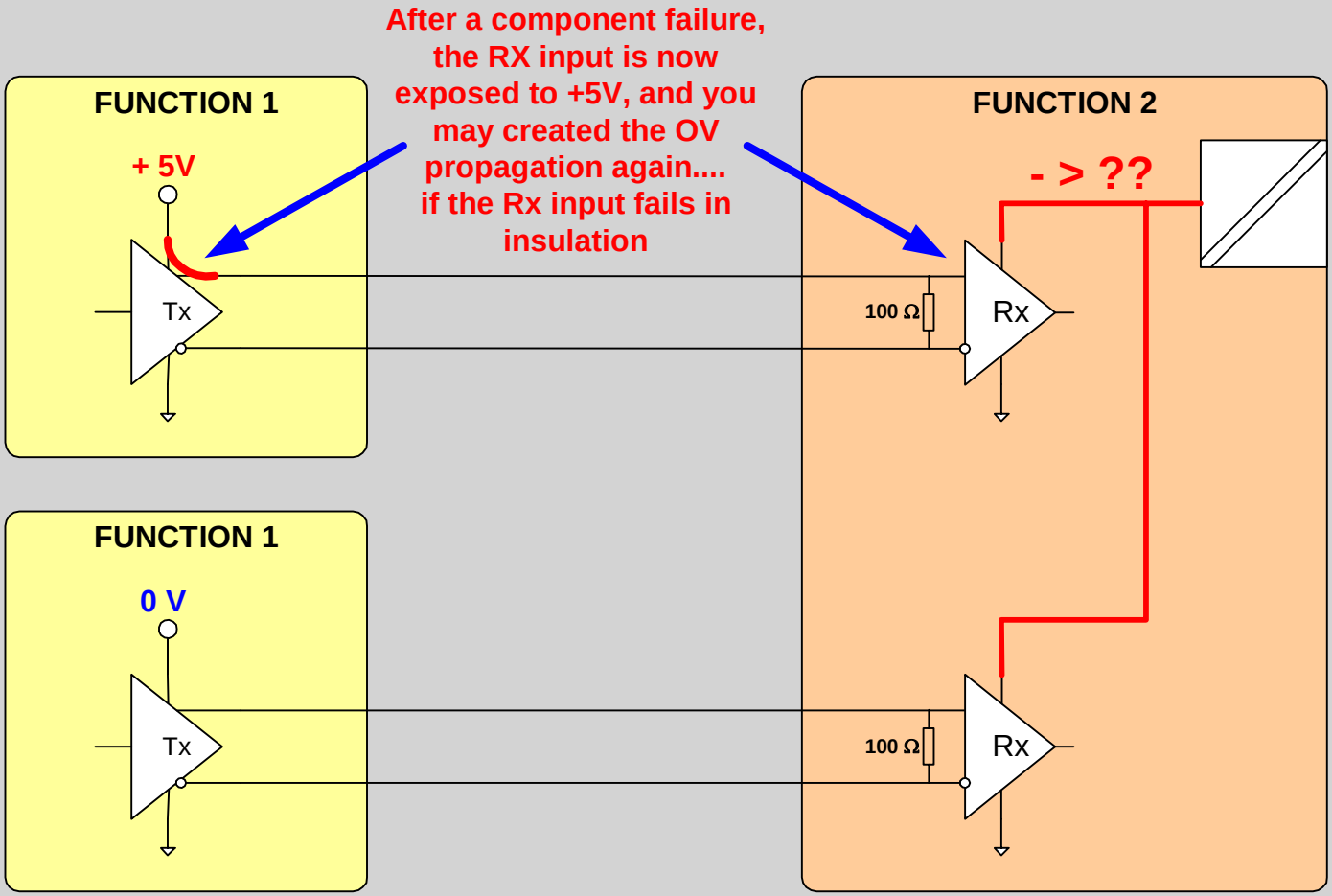
- ALL POWERING OF EXTERNAL (LVDS) I/F CIRCUITRY IN A SYSTEM X-COUPLING, SHALL BE OVER-VOLTAGE PROTECTED BELOW THE CIRCUIT'S "ABSOLUTE MAXIMUM VCC RATINGS"

POWERING LVDS WITH DIFFERENT VCC

- The Creative engineer uses a +5.0V LVDS Tx with a +3.3V Rx circuitry. He discovered that it works on the lab, because we have a current-mode interface.

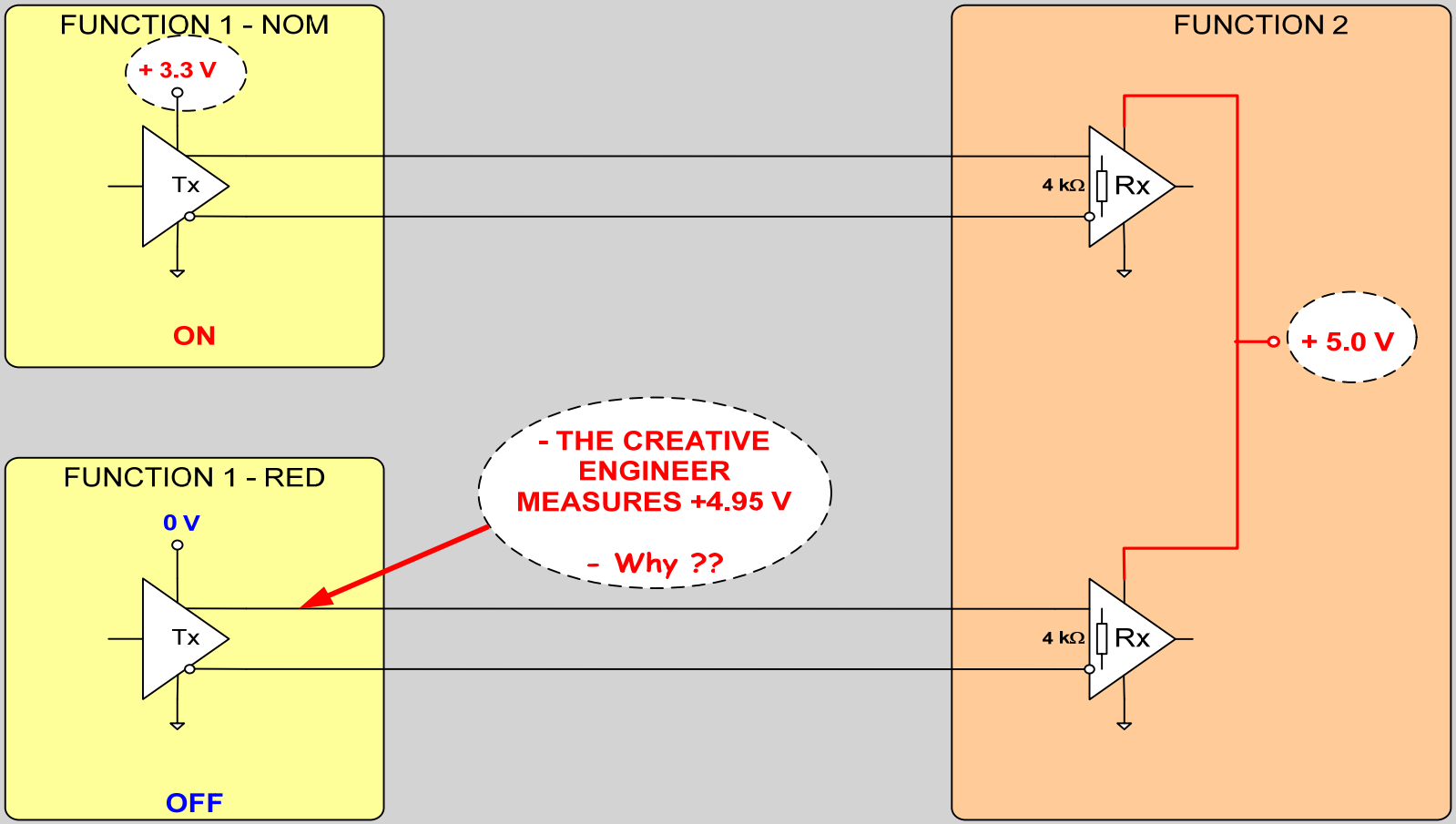


BUT WHAT HAPPENS IF THE +5V LVDS FAILS…?

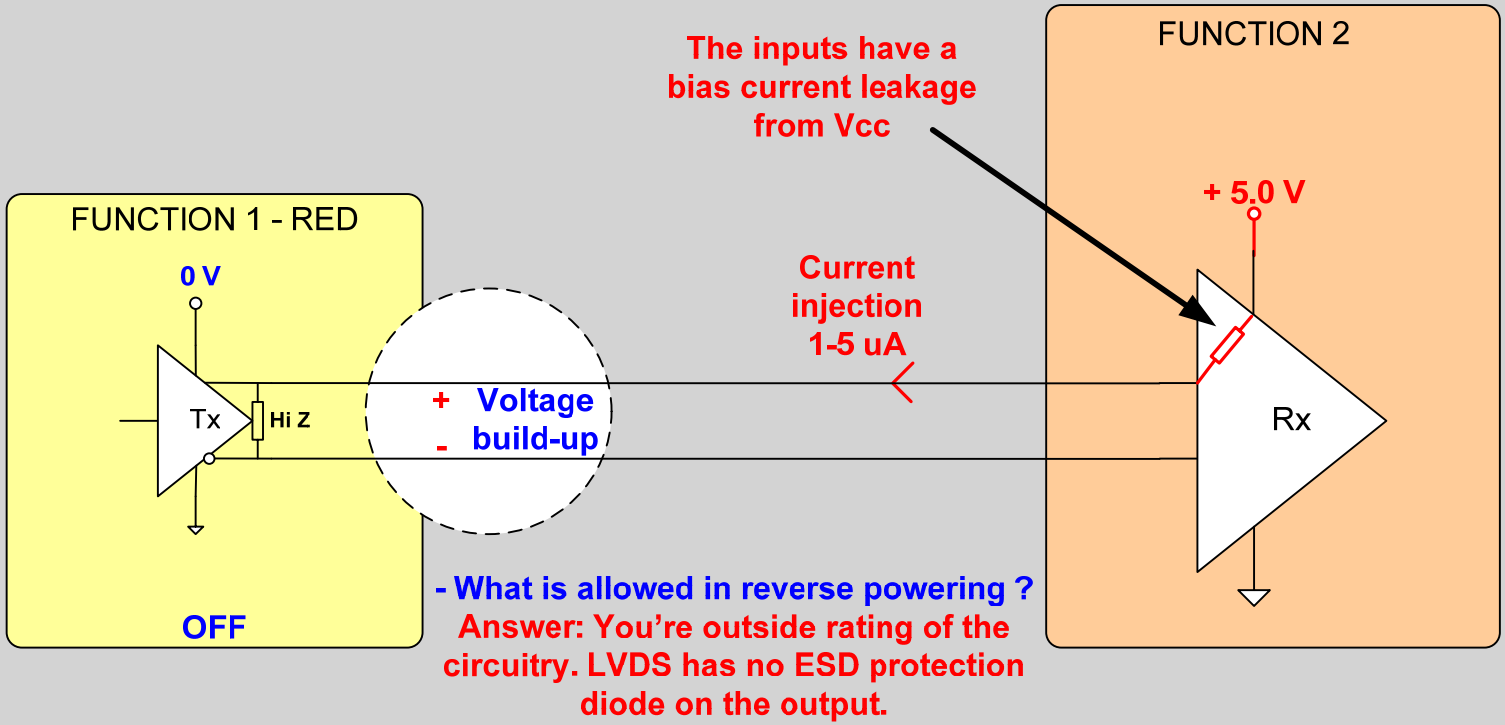


HOW IS A RS422 Rx AFFECTING A NON-POWERED LVDS Tx ?

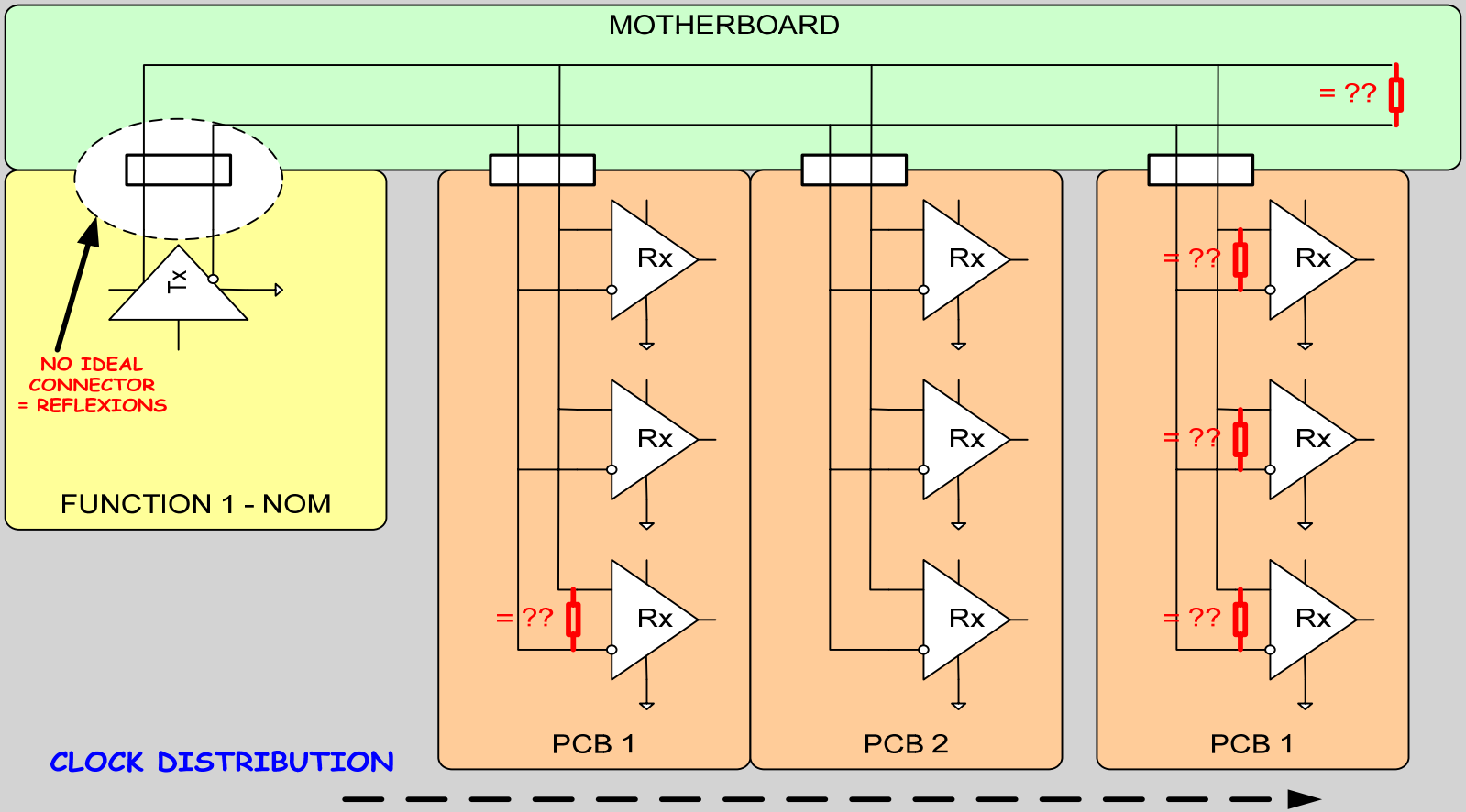
- The Creative engineer uses a +3.3V LVDS Tx with a +5.0V RS422 Receiver, because we have a current mode I/F…….and is "seems to work" with the input impedance of RS422



- Any receiver circuitry always have a leakage from the input terminal



- BY TRYING TO IMPLEMENT MULTI-DROP OVER A BACKPLANE, YOU ARE INTRODUCING MANY POTENTIAL PROBLEMS – REFLEXION DIAGRAM WILL BE EXTREMELY COMPLICATED !!!



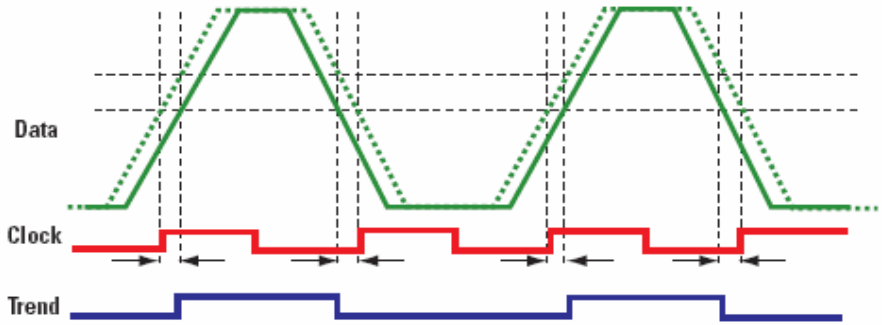
PLEASE DON'T DO THIS – USE POINT-TO-POINT DISTRIBUTION !!

THE POWER QUALITY AND CIRCUIT DECOUPLING IS VERY IMPORTANT FOR A HIGH PERFORMANCE LVDS INTERFACE!

- Let us assume that we want to achieve a high frequency clock (> 20 MHz) with an extremly good scew / jitter performance.

- The LVDS manual from National Semiconductor tells us this.....

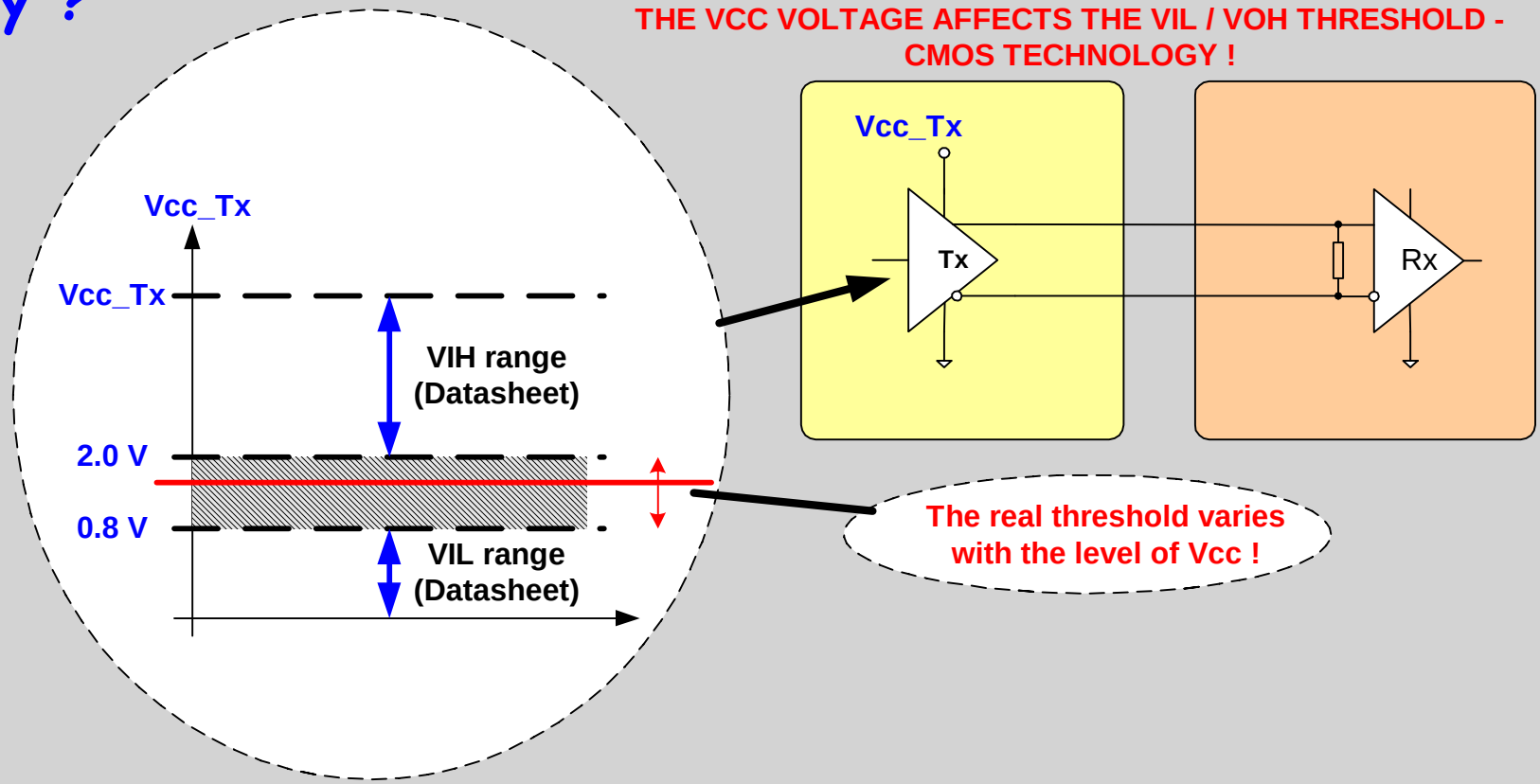
The waveform represented by the dotted line in *Figure 6-3* shows the ideal output of a transmitter with an accurate threshold level set at 50% and with a duty cycle of 50%. The solid line waveform represents a distorted output of a transmitter due to a positive shift in the threshold level. With a positive shift in threshold level, the resultant output signal of the transmitter will have less than 50% duty cycle. If the threshold level is shifted negatively, then the output of the transmitter will have greater than 50% duty cycle.



..... but what does it mean to US?

- It really means that the power supply at Vcc must be stable !

- Why ?



Conclusion

THE HAPPY ENDING

Taking into account the provided recommendations in this presentation for SpaceWire Links X-COUPLING

THE SYSTEM SpW-BASED ENGINEER'S BLESSING

THE POWER ENGINEER'S BLESSING