

20th, Feb. 2008



Recent ASIC Developments by NEC

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Space Cube Architecture - a mutual subset of T-Engine architecture (1)

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□ from Palm-top size reference model through chip-size implementation



Space Cube



Space Cube 2

developed in 2005

Space Cube Architecture

- Joint development with JAXA/ISAS

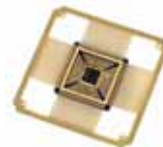


Space DICE



Space Cube MCM
(Chip-size assembly)

under development

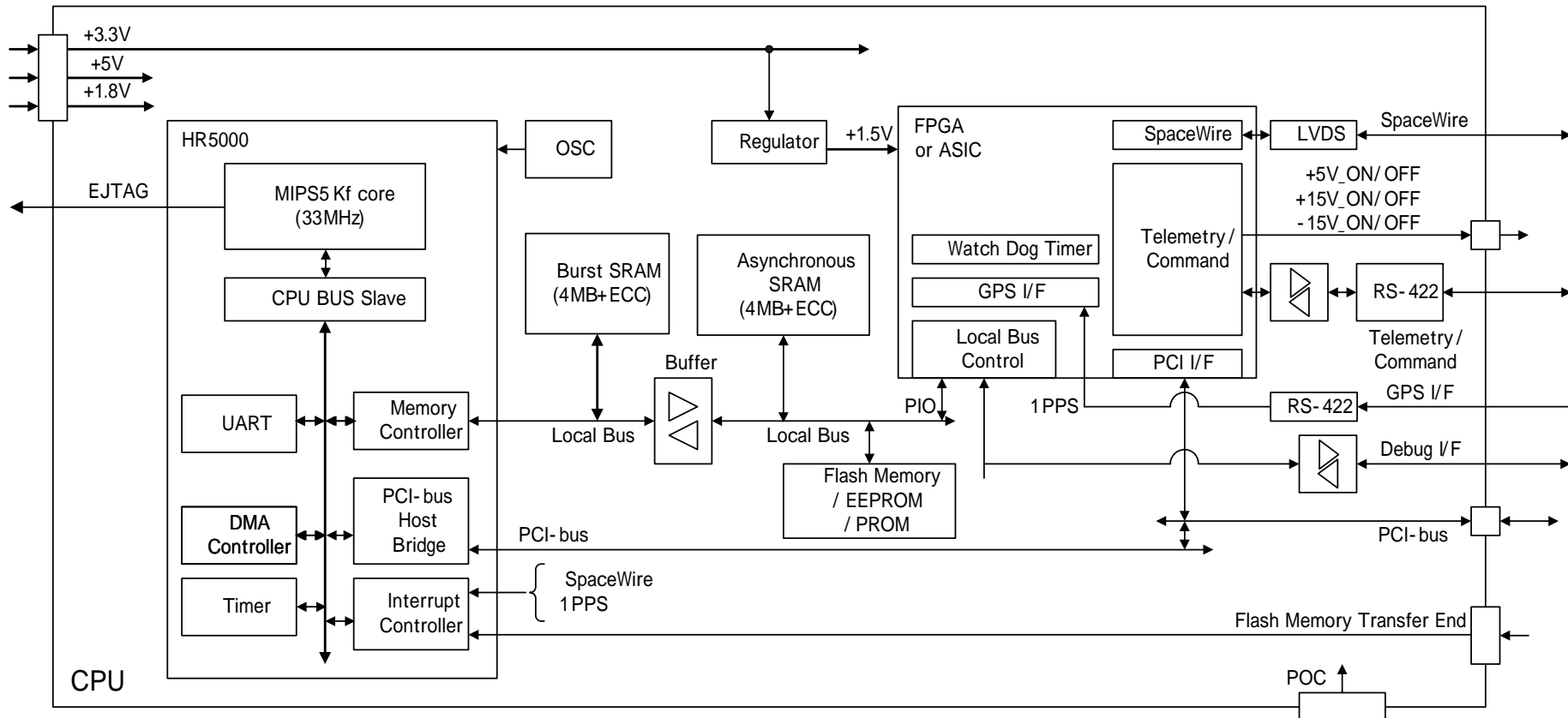


Space Cube Chip . . . Goal !

Space Cube Architecture - a mutual subset of T-Engine architecture (2)



Basic CPU module for Space Cube 2



Space Cube® 2 - Technical Features

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□ Base Model

- SpaceWire interface: 3ch
(additional ports are available)
- UART interface: 2ch @ RS422
- System Memory:
 - FLASH Memory (2MB) and/or PROM/EEPROM
 - Burst SRAM (4MB)
 - Asynchronous SRAM (4MB)
- Data Recorder Memory:
 - SDRAM (1GB)
 - Back-up FLASH Memory (1GB)
- Size (mm): 71(W) x 220.5(D) x 175.5(H)

Key ASICs for Space Cube 2

64bit MPU and Burst SRAM developed by JAXA

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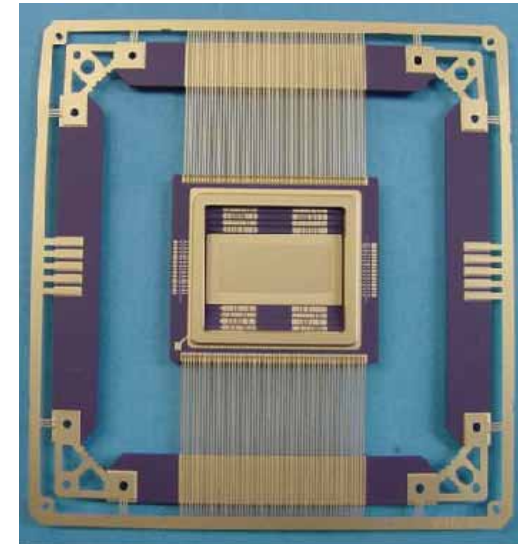
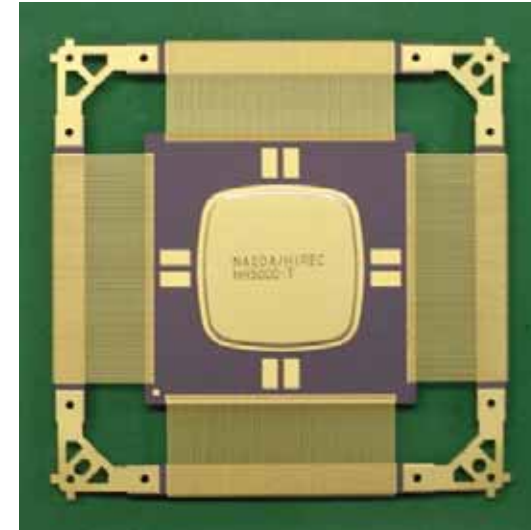


□ HR5000

- 320MIPS 64bit micro-controller with integrated peripheral devices on one chip
- 0.18 μ process
- Peripherals
 - PCI Ver. 2.2
 - eight-bank memory controller with EDAC
 - 2ch UART
 - 2ch Timer
 - 2ch DMA controller
 - Interrupt controller

□ Burst SRAM

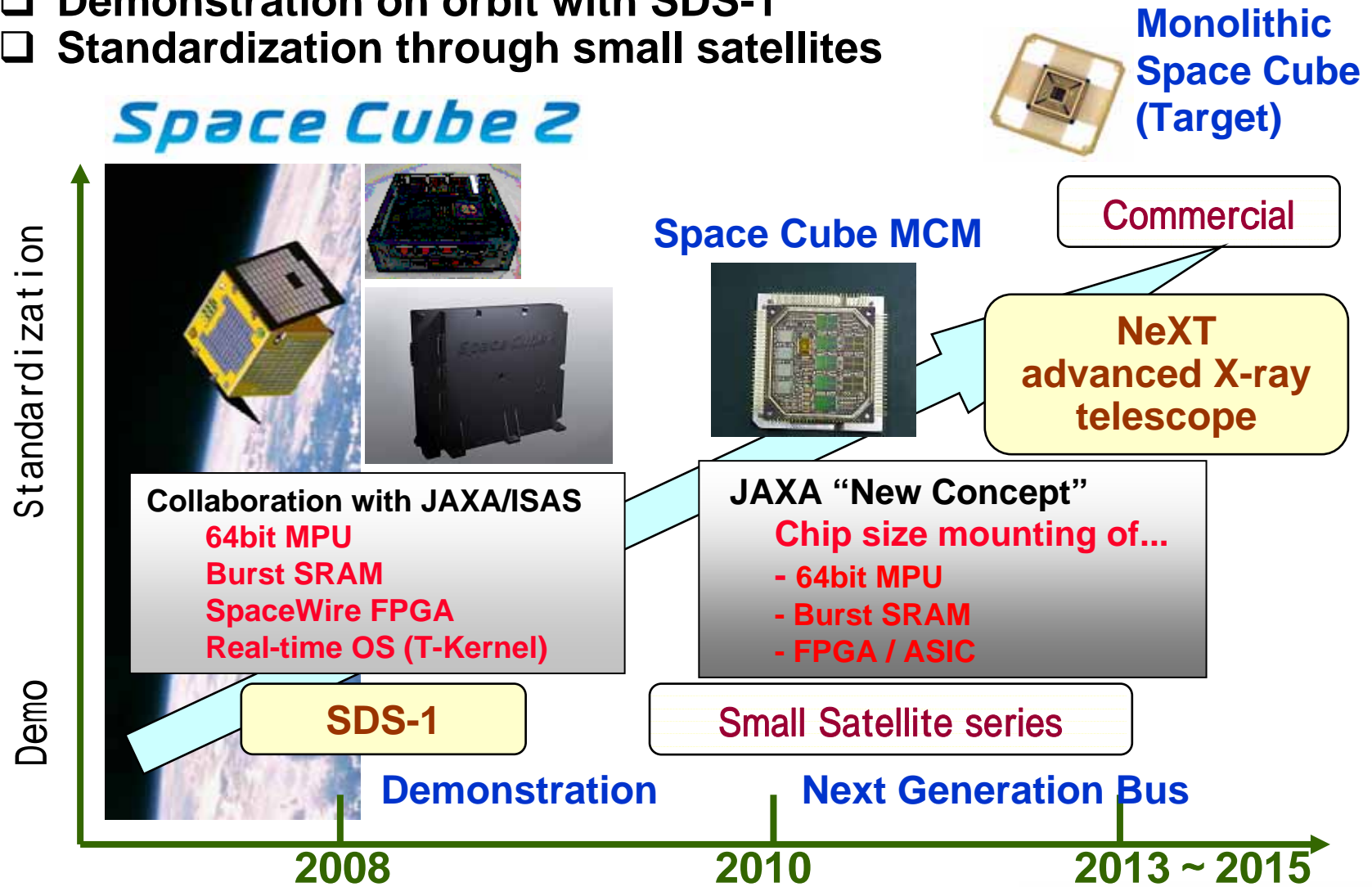
- 36Mbit / chip



Road Map Overview for SpaceWire in Japan



- ❑ Demonstration on orbit with SDS-1
- ❑ Standardization through small satellites

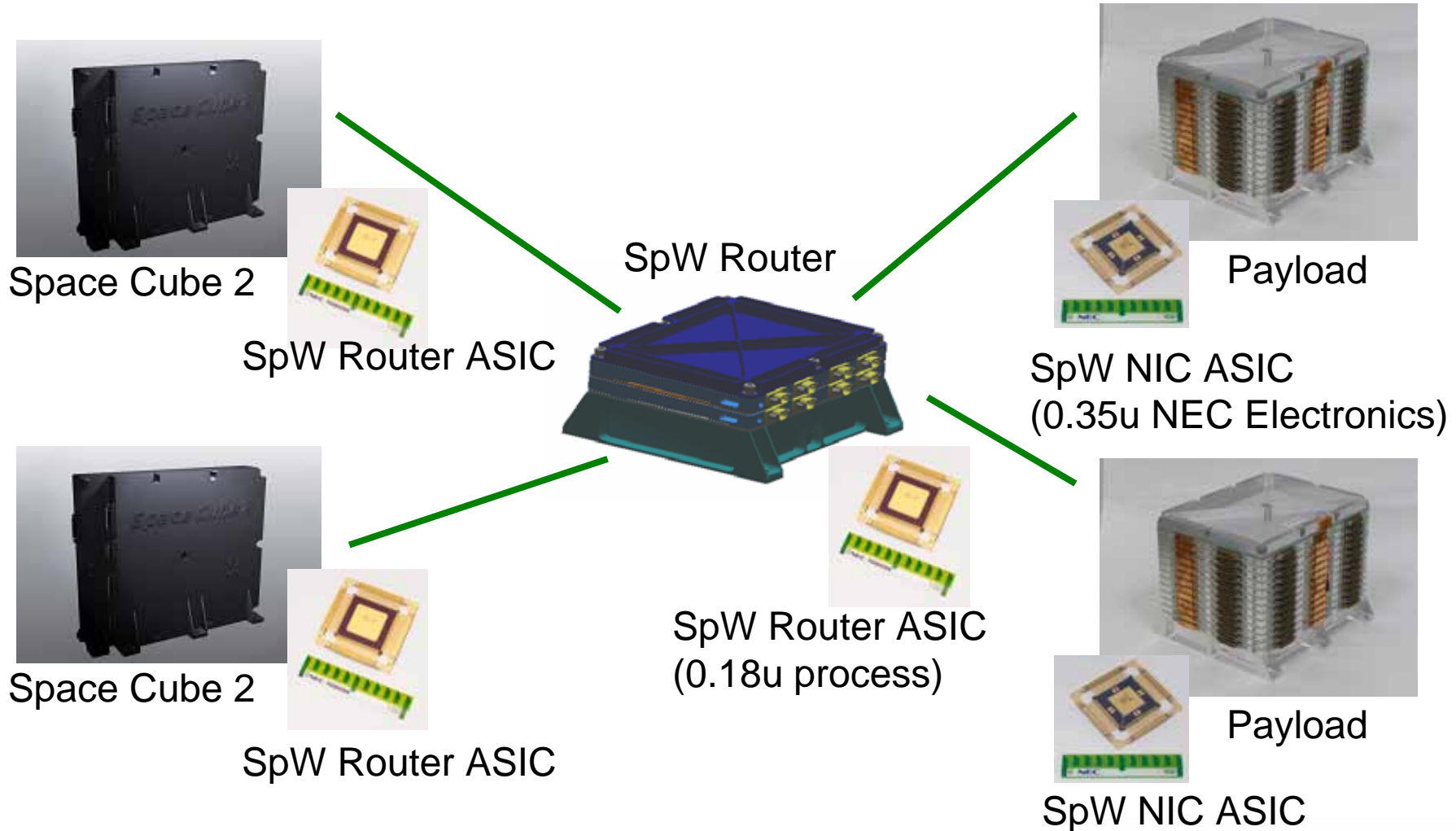


Satellite Assembly Kit with SpaceWire ASICs for standardized satellite bus

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□ Space Cube 2, Router ASIC, and NIC ASIC



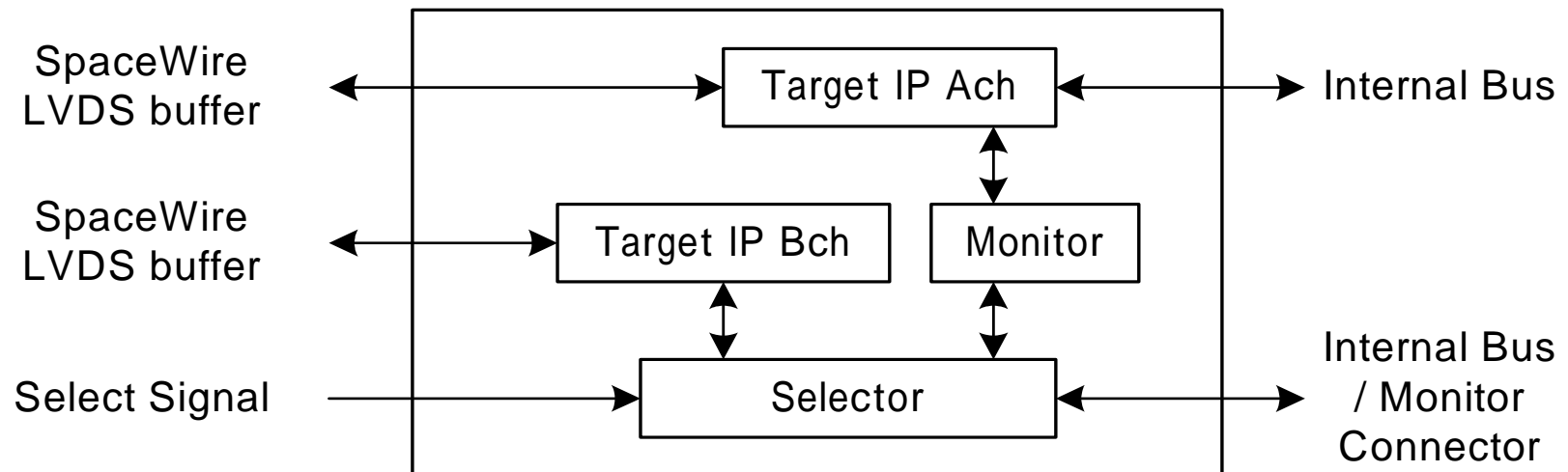
User-side SpaceWire interface ASIC - SpaceWire-NIC07

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□ Common network interface chip for components

- Two SpaceWire ports
- Selectable Monitor Function

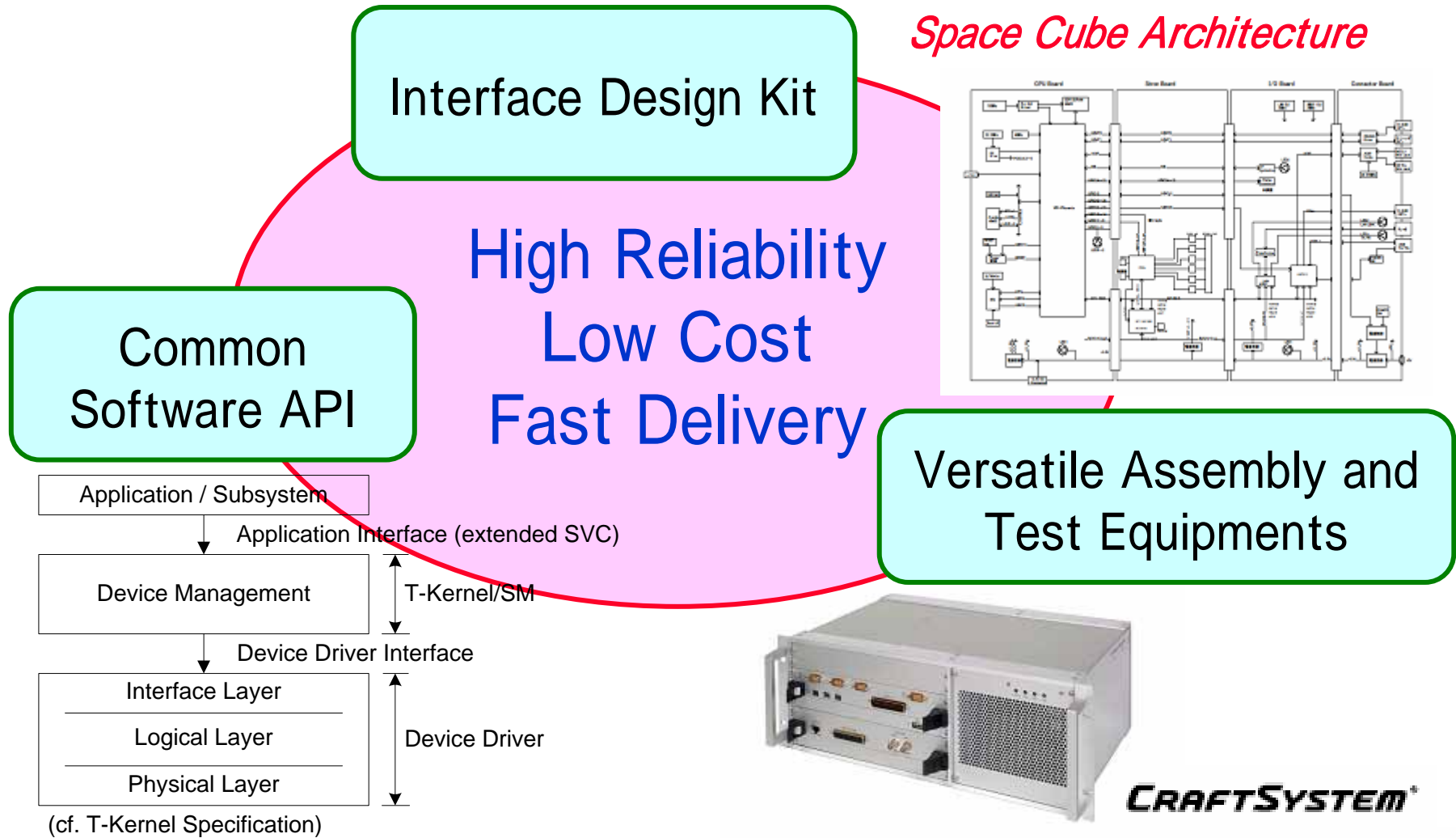


Platform extension for exploiting SpaceWire ASICs

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❑ Support system for development



Common Software Interface for SpaceWire ASICs

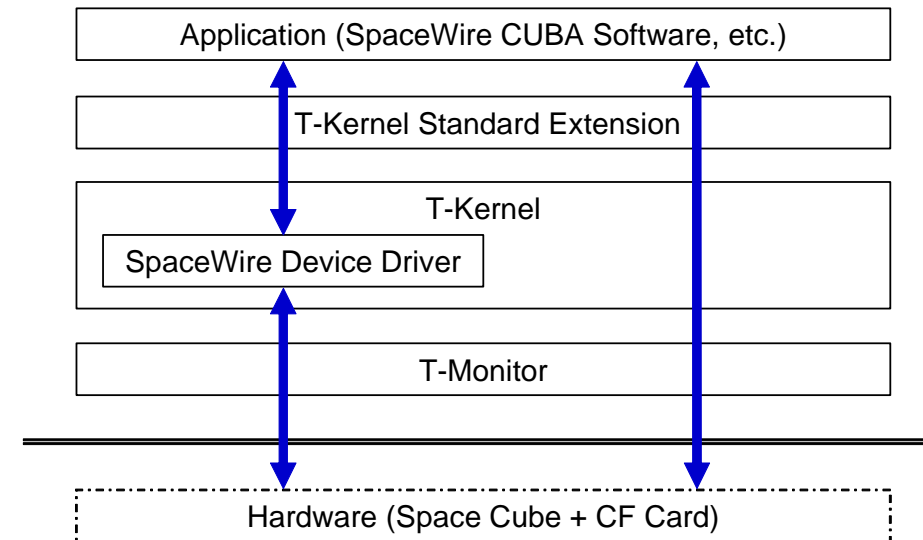


❑ Common API with UoD

- developed in joint development activity

❑ T-Kernel

- State-of-the-Art real-time operating system
- the successor of TRON operating system, developed in TRON project
- standardized by Ubiquitous Networking Laboratory, Tokyo.



Reference Software Architecture
on Space Cube

Test equipments for developing components using SpaceWire ASICs



□ SpaceWire test set with legacy interface support



SpW USB Brick



Conformance Tester



SpW Link Analyser

by STAR-Dundee

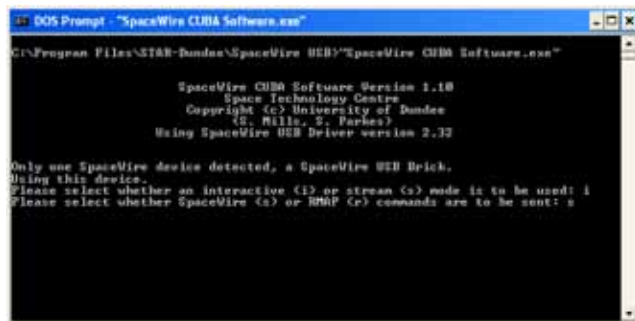


(RG408-L platform)



Multi-link SpaceWire Analyser
(Plug-in memory card defines the ESL function)

Multi-Link SpW Analyzer by 4Links



SpW CUBA Software with Space Cube by UoD and NTSpace



CRAFTSYSTEM®

Multi Protocol Tester with SpW and Legacy I/F by NEC/NTSpace

SpaceWire CUBA Software

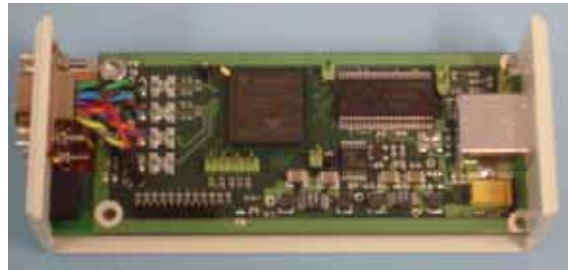


- The same RMAP protocol analyzer software runs on both USB brick and Space Cube®

Common API is established



USB brick



SpaceCube®

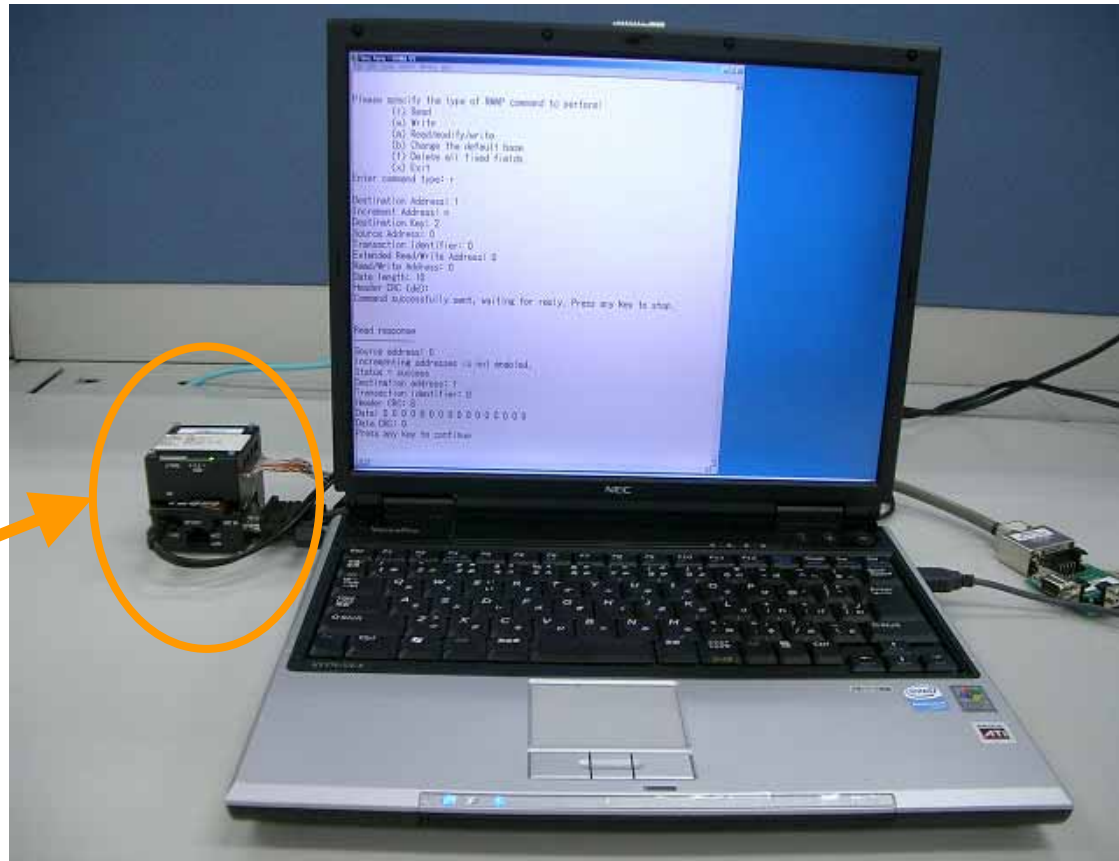
Portable Test Set for SpaceWire / RMAP

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□ SpaceWire CUBA Software on Space Cube

Space Cube



Onboard software development Platform using SpaceWire ASICs

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❑ SOFTWARE DEVELOPMENT ENVIRONMENT

- Commercial level Space Cube®-mini
 - Engineering model with HR5000 micro-controller



- Palm top size model (original Space Cube®)
 - VR5701 (commercial 64bit micro-controller by NEC Electronics Corp.)



- JTAG ICE (In-circuit Emulator) by Yokogawa-Digital Corp.



SpaceWire User's Group, Japan

-- User support community for SpW application

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□ SpaceWire User's Group Constitution

- Chair
 - Prof. T. Takahashi (JAXA/ISAS)
 - Prof. M. Nomachi (Osaka University)
- Founder Members
 - JAXA/ISAS
 - NEC TOSHIBA Space Systems, Ltd.
 - NEC Electronics Corp.
 - NEC Soft, Ltd.
 - Sumitomo Heavy Industries, Ltd.
 - Mitsubishi Heavy Industries, Ltd.
 - Meisei Electric Co., Ltd.
 - NIPPI Corp.

