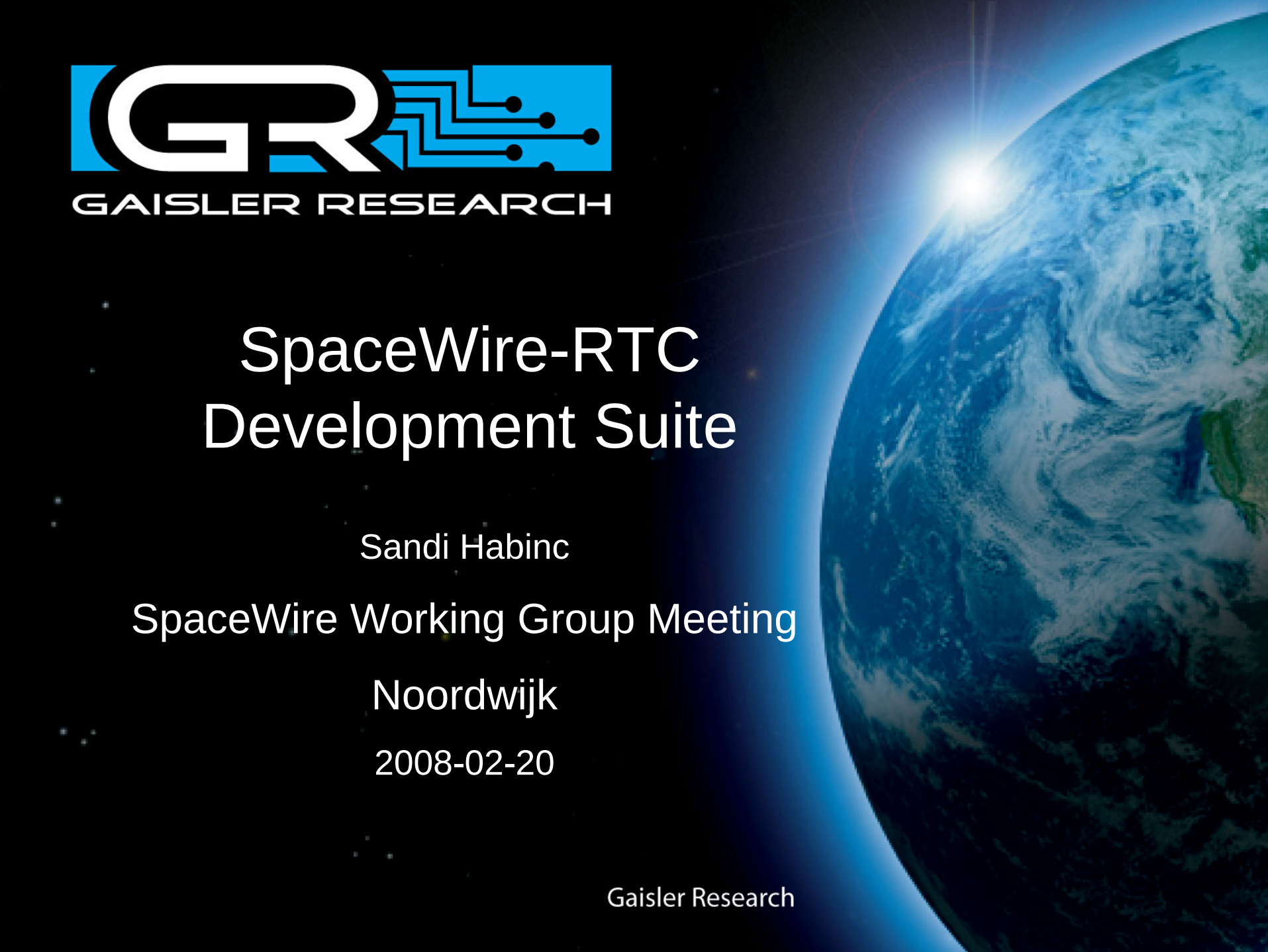

SpaceWire-RTC Development Suite

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SpaceWire Working Group Meeting

Noordwijk

2008-02-20

SpaceWire-RTC Development Suite

Hardware:

- ASIC development board
- ASIC development board with encasement
- ASIC development board with cPCI front-panel
- FPGA development board

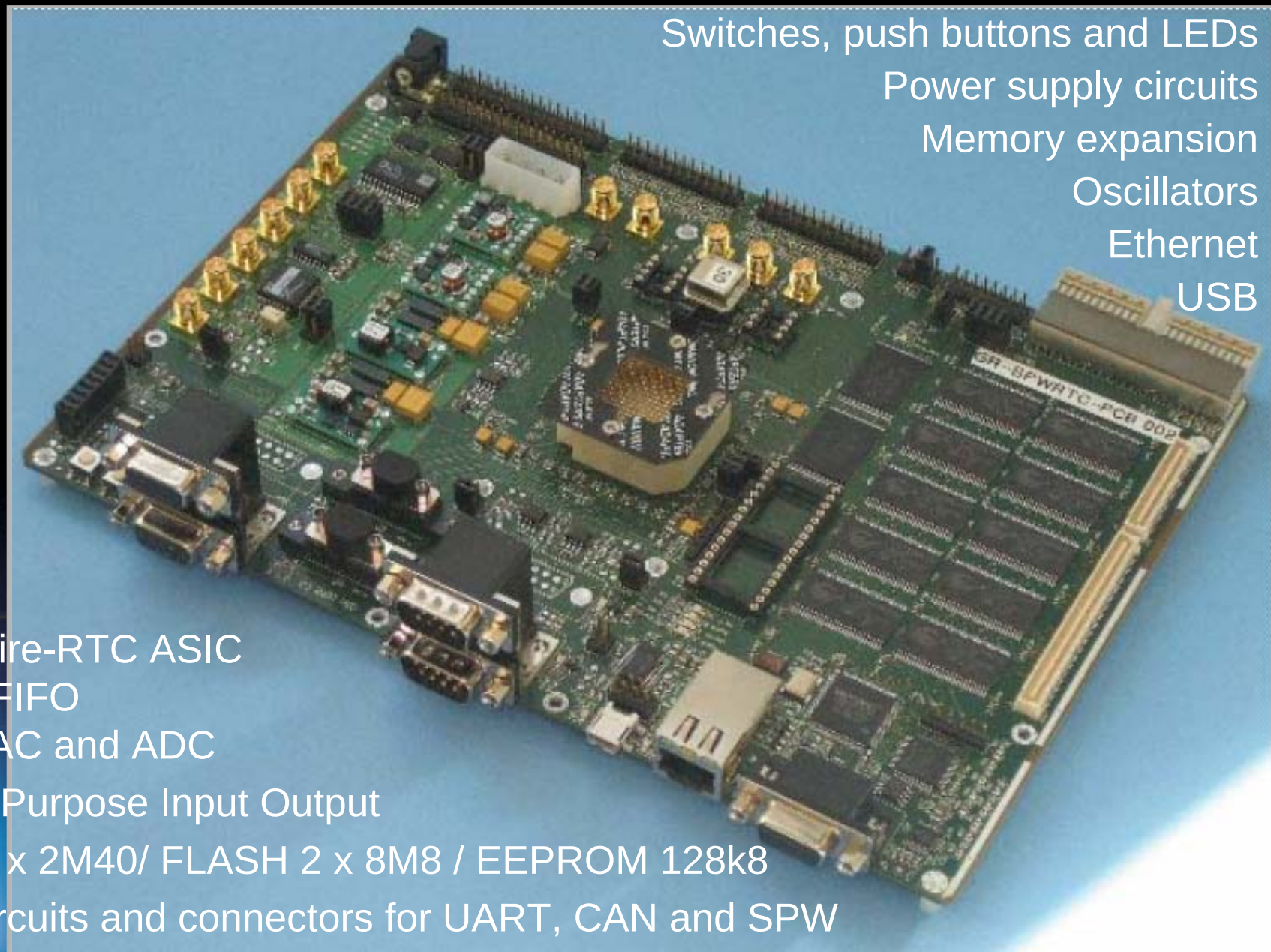
Software:

- Bare-C compilation system (BCC)
- RTEMS – drives and BSP
- Wind River VxWorks – drivers and BSP

Tools:

- GRESB – Ethernet SpaceWire bridge
- GRMON – debug monitor
- TSIM2 – instruction simulator with loadable module

SPW-RTC ASIC – board



Switches, push buttons and LEDs
Power supply circuits
Memory expansion
Oscillators
Ethernet
USB

SpaceWire-RTC ASIC
8/16 bit FIFO
12-bit DAC and ADC
General Purpose Input Output
SRAM 2 x 2M40/ FLASH 2 x 8M8 / EEPROM 128k8
Driver circuits and connectors for UART, CAN and SPW

SPW-RTC ASIC – box

GAISLER RESEARCH

SPW-RTC ASIC – box opened

GAISLER RESEARCH

SPW-RTC ASIC – box opened

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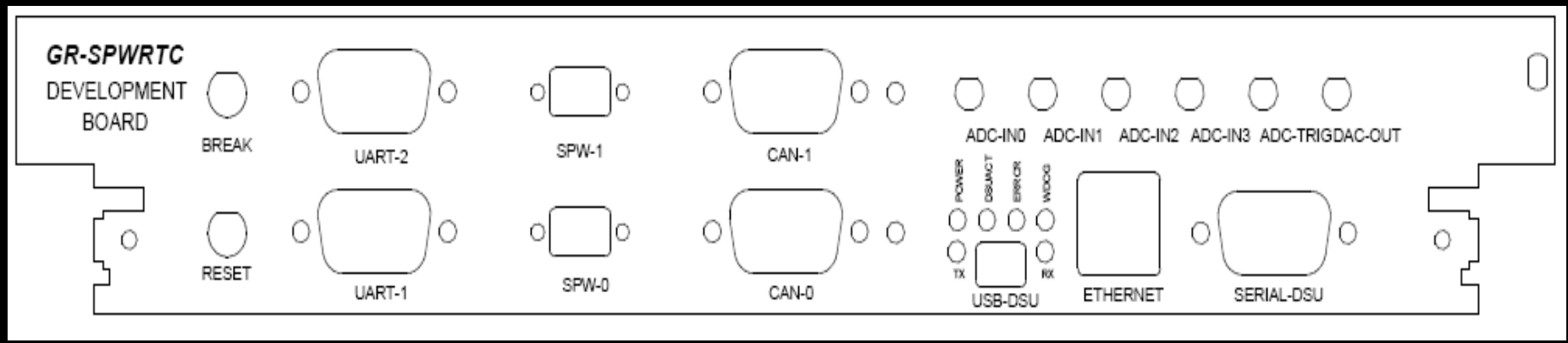
SPW-RTC ASIC - CPCI 6U

SPW-RTC ASIC - CPCI 6U front panel



SPW-RTC Development Suite - Software

Existing RTEMS 4.6.5 and VxWorks 6.5 LEON2 support:

- LEON2-FT Integer Unit with MEIKO Floating Point Unit
- LEON2 Memory Interface
- LEON2 Debug Serial Link UART
- LEON2 General Purpose Input Output & UART Serial Links
- LEON2 32-bit Timer
- LEON2 Interrupt Controller

New SpaceWire-RTC ASIC drivers, data structures and functions:

- FIFO Interface
- CAN Interface
- SpaceWire Link Interface
- LEON2 Secondary Interrupt Controller
- On-chip Memory
- 32-bit Timers
- 24-bit General Purpose Input Output
- ADC/DAC Interface

TSIM2 – LEON2/3 instruction simulator

TSIM2 Loadable Module for SpaceWire-RTC ASIC emulation:

- SpaceWire interfaces, with DMA and RMAP
- CAN bus interface, with DMA
- FIFO interface, with DMA
- ADC / DAC interface
- 32-bit Timers, 24-bit GPIO, On-Chip Memory
- LEON2-FT 16-bit GPIO and Secondary Interrupt Controller

Not emulated:

- Debug Support Unit, Debug Serial Link UART

High level of data abstraction:

- SpaceWire packets, CAN messages, block of FIFO data

Fidelity of emulation allows:

- RTEMS and VxWorks simulation
- Repetition of FPGA/ASIC validation

Rich and flexible user interface allows:

- Emulation of surrounding board/system, socket usage