SMCS116SpW - AT7912E
In Advance Information on Anomalies

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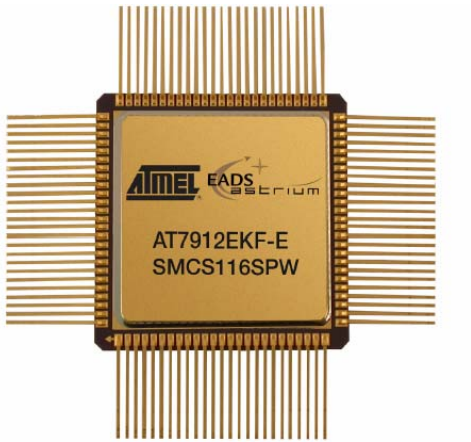
Onboard Payload Data Processing section (TEC-EDP)



Outline

- Main Characteristics of the SMCS116SpW
- Background
- Typical Application Areas
- Anomalies
- Description and Solution of Anomalies
- Ongoing and Upcoming Activities

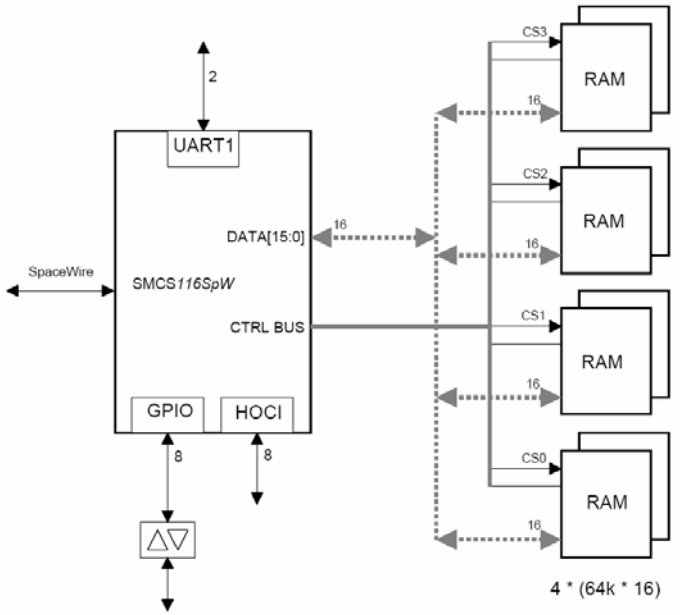
Main Characteristics of the Chip

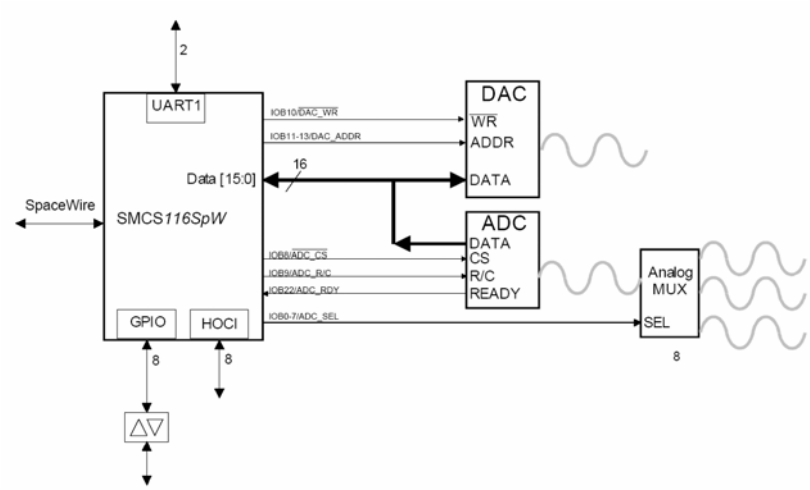
- Interfaces one SpW link to various interfaces such as ADC/DAC, RAM, FIFOs, GPIOs and UARTS
- MQFP 100 pins package
- Supports both 5V and 3.3V operation
- SpW link speed: 200Mbps@5V, 100Mbps@3.3V
- Support Serial Universal Protocol (STUP)
  - Supports use in a SpaceWire network with distinct protocols
- Power consumption: 0.7W@5V, 0.4W@3.3V
- 0.5um MG2RT (ATMEL) CMOS technology
  - Total dose tested up to 50Krad
  - No SEL at 70 MeV/mg/cm2
  - SEU hardened flip-flops
- Engineering Models: Available
- Flight Models: order entry open

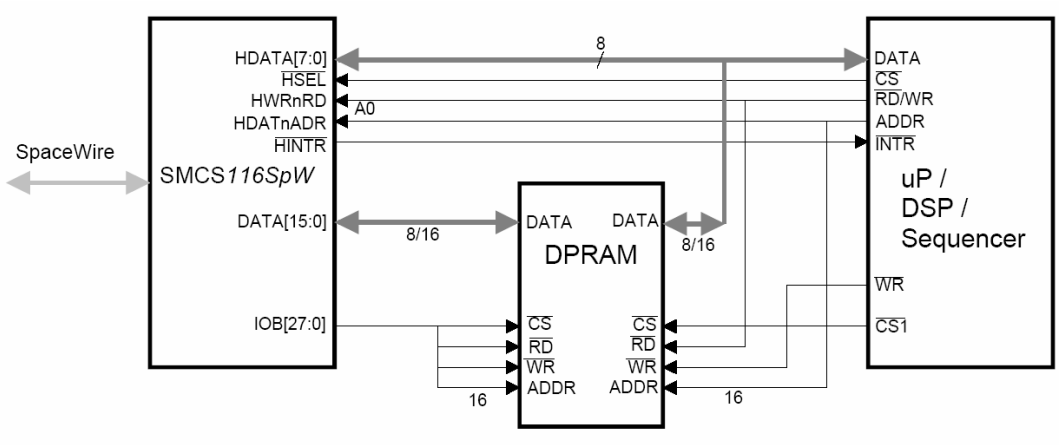
Background

- The first generation of the SMCS116 and SMCS332 high speed digital links controllers is based on the IEEE1355 standard.
- In order to be make them fully compliant to the SpW standard an activity was launched upgrade these two devices.
- In addition known anomalies where fixed and enhanced features where added as well as migrating to at that time latest silicon technology MG2RT.

Typical Application Areas for the SMCS116SpW







SMCS116SpW Anomalies

- Three anomalies have been identified
  - The first reported anomaly effects the reliable reception of data with the SMCS116SpW
  - The second reported anomaly is related to the behavior of the “packet header enable” function
  - The third reported anomaly is related address line 15 of the RAM I/F only driving low voltage.
- The anomalies will be described in the following slides

Description of Anomaly #1

- Due an anomaly in the receive section in the SpW cell of the SMCS116SpW an invalid FCT character is generated allowing the other node to send more data which cannot be processed and thus gets lost due to this reason.
- The anomaly is NOT related to the SpW codec but to the design of an internal FIFO of the SMCS116SpW.
- The loss of data can be avoided if the receive data rate on the SpW link is lower than the rate with which the data are written to the memory
- The anomaly can be corrected by with changes at gate level logic.

Description of Anomaly #2

- When packet header insertion is enabled in some cases it can occur that at the end of the packet being transmitted, the packet header will be appended again.
- This is caused by an erroneous state machine in the transmit control logic between the interfaces and SpW cell.
- Proposed correction of anomaly is based on minor changes to the gate level logic

Description of Anomaly #3

- Using the RAM I/F; the ram address line 15 drives only low voltage. The signal for the ram address line 15 is shared with the FIFO control signal *rcvd_eopl* from the FIFO I/F
- Due to a missing description in the VHDL code the proper multiplexing was not realized.
- Proposed correction of anomaly is based on minor changes to the gate level logic

Anomaly Correction

- Ongoing Validation Tests
- Perform changes to the EDIF netlist
- Verification of the modified design
  - Formal verification
  - Static timing analysis
- Anomaly correction by ASIC re-run
- Planned start is end of Q1
- Delivery of prototypes: T0 + 11 weeks
- Completion of prototype tests: T0 + 14 weeks

Thank you
for
your attention

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