SpaceWire Router ASIC : SpW_10X - AT7910E

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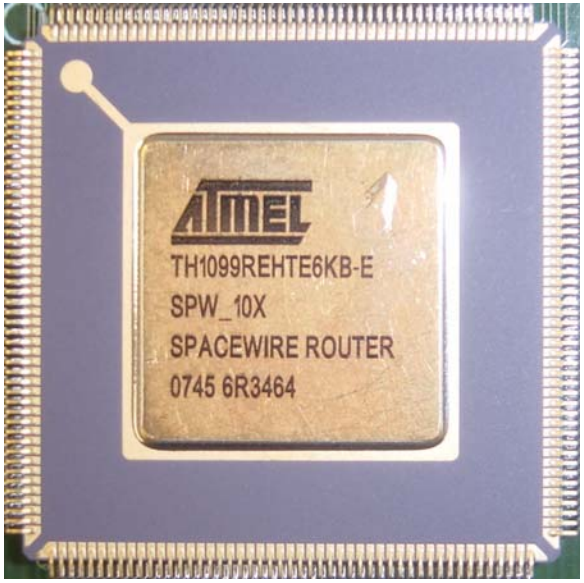


Main Characteristics of the chip

- MH1RT 0.35 CMOS with latch-up immunity up to 80 MeV/mg/cm2,
- 196 pin ceramic Multilayer Quad Flat Package (MQFP)
- 8 full duplex SpW serial links (2-200 Mbps) with LVDS Tx / Rx
- Cold sparing LVDS buffers,
- 2 two external parallel ports,
- 1 internal RMAP configuration port (routing table, priority scheme, status and configuration registers),
- Low latency, non-blocking, worm-hole, group adaptive router,
- Logical and Path addressing, Priority schemes, timeouts …
- Low power consumption w.r.t. to data rates
- Manages and distributes time-codes (network synchronization),
- External time-code and status signals,
- Very comprehensive and detailed user manual (written by UoD)
  - at http://spacewire.esa.int/content/Home/HomeIntro.php
  - With guide for typical user applications
  - With numerous illustrations of features : priority example
  - With warnings all along the document and a warning section

Validation activities

- Design extensively validated on FPGA platform
- ASIC taped out in **October 2007**
- Among 20 ASIC for ESA only 8 are unused yet
- **Functional validation task (ASTRIUM)** completed last week with very good results and just 2 small findings :
  - Tri-state mode in combination with failsafe resistor network
  - Chip RESET while SpW links are running
- **Electrical characterization activity (AAE)** (links speed, power consumption, output D-S skew, clock signals, eye diagrams, PLL function) under temperature (-55ºC, +25ºC, +125ºC) and load stress
- **SpaceNet SpW_10X testing (UoD, Wahida Gasti):** test traffic load stress, boundary cases, throughput, operation in various configurations for FDIR purposes.

Upcoming Dates

- **ASIC Validation (ASTRIUM within the main activity)** :
  - ASIC Validation Review on **25.02.2008**
- **ASIC Characterization activity (Austrian Aerospace) :**
  - Start of Measurements on **01.03.2008**
  - All measurements and test results available by **end of May 2008**.
- **Flight parts** :
  - Prototype approval expected by **25.02.2008**
  - 1 month later **AT7910E preliminary data sheet** on ATMEL website
  - then customers can order flight parts to ATMEL
  - 3 to 6 months for delivery depending on QML-V, QML-Q or EQML.

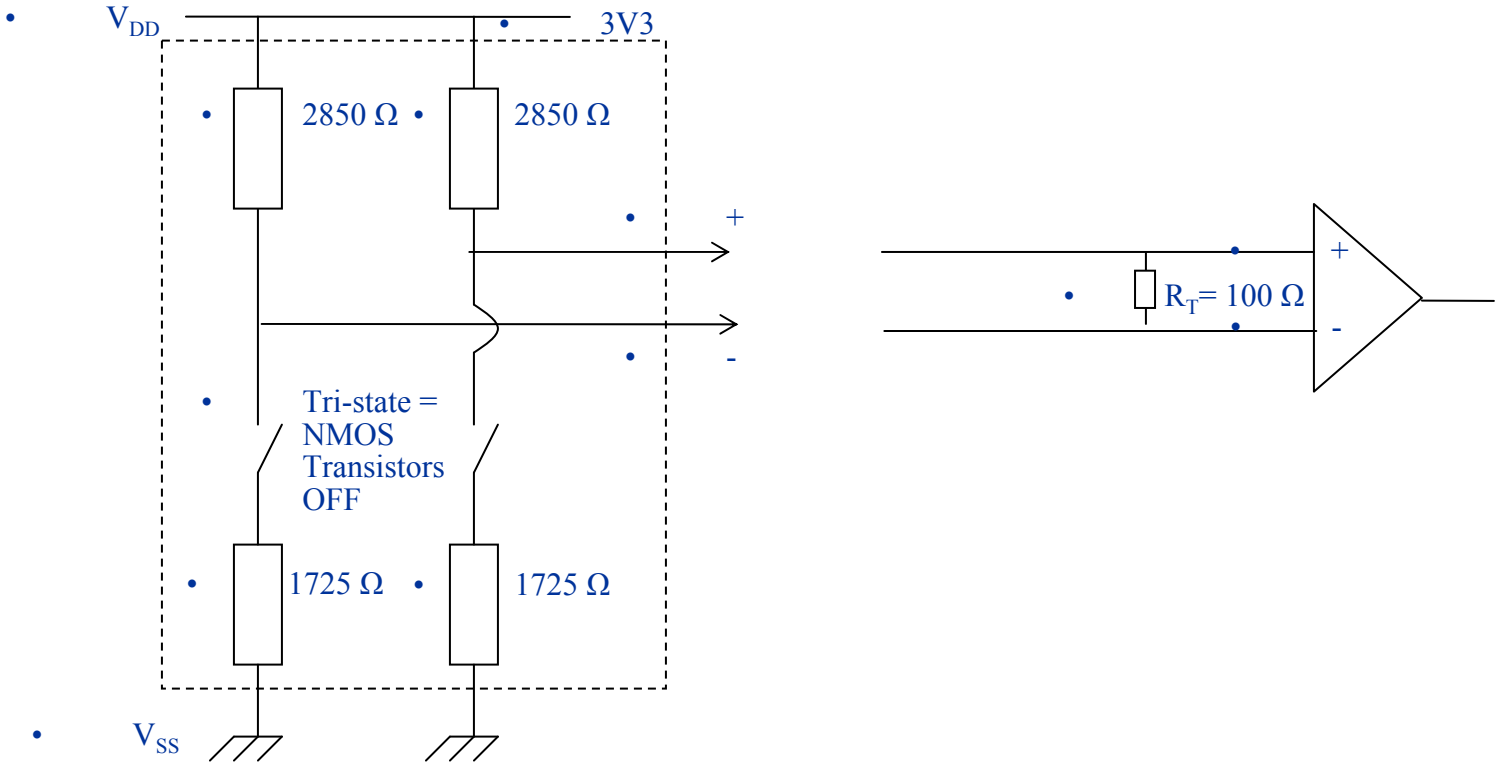
Thank you
for
your attention

For Further Information Contact

SpaceWire.Components@esa.int

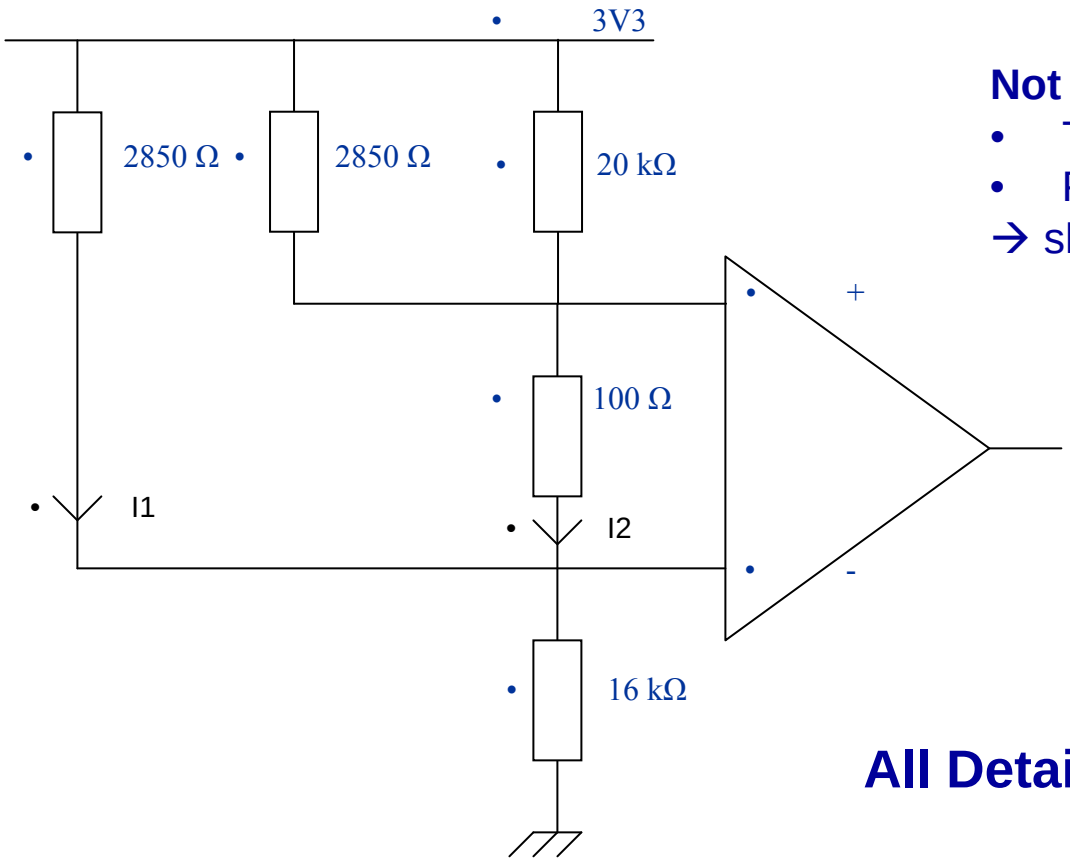
Tri-state mode without failsafe resistor network

- Without failsafe resistor at LVDS Diff Input → at the other side of the link LVDS Drivers can effectively be tri-stated (high impedance, no power consumption)



Tri-state mode with failsafe resistor network

With Failsafe resistor network (used to avoid that PCB tracks - or connectors/cables of a disconnected input pick-up EMI noise and trigger the receiver input in series of 0 and 1 that will potentially start up a fake link …).



Not a pure tri-state mode:

- Total current : **190 µA**
- Power : **0.627 mW**

→ shall be called **"deactivated mode "**

All Details to be in the user manual !

Chip RESET while SpW links are running

If SpW links are running then :

- **When reset is activated (high-to-low)** :
  - D & S hold their previous values on the output ports until reset is released,
  - a glitch may occurs on D & S on the output ports.
- **When reset is released (low-to-high)** :
  - part of a NULL may be generated on the output ports,
  - Simultaneous transitions may happen on the output ports.

Proposed solution : if the whole network is sensitive (presence of a sensitive CODEC) to the RESET effects of an active router → first isolate that router by use of the link-disable commands and then reset!

Draft TN → **will be documented in user manual !**

10.6.5 Time-code Jitter

The variation in time to propagate a time-code through a routing switch.

Time-code jitter occurs in the synchronisation handshaking circuits and the transmitter where the maximum delay time the time-code has to wait to be transmitted is one data character. The jitter is measured as

$$T_{TCJIT} = (2 \times T_{SYSPERIOD}) + (5 \times T_{TXPERIOD})$$

10.6.6 200M bits/s Input and Output Bit Rate Example

The following table defines the latency and jitter measurements when the transmit bit rate and receive bit rate are 200M bits/s.

Table 10-6 SpaceWire Router Latency and Jitter Measurements (Bit rate = 200Mbits/s

Description	Symbol	Value	Units
Switching Latency	T_{SWITCH}	133.3	ns, max
Router Latency – SpaceWire to SpaceWire port	T_{SSDATA}	546.6	ns, max
Router Latency – SpaceWire to External port	T_{SEDATA}	316.6	ns, max
Router Latency – External to SpaceWire port	T_{ESDATA}	363.3	ns, max
Router Latency – External to External port	T_{EEDATA}	166.6	ns, max
Time-code Latency – SpaceWire to SpaceWire port	T_{SSTC}	409.3	ns, max
Time-code Latency – SpaceWire to External port	T_{SETC}	316.6	ns, max
Time-code Latency – External to SpaceWire port	T_{ESTC}	359.9	ns, max
Time-code Jitter	T_{TCJIT}	116.6	ns, max

[1] Note all figures are worst case

11. ELECTRICAL CHARACTERISTICS

The electrical characteristics for the SpaceWire router are defined in this section

11.1 DC CHARACTERISTICS

The operating conditions are listed in Table 11-1. For a detailed list of the operating conditions see [AD3].

Table 11-1 Operating Conditions

Symbol	Description	Value	Units
V_{DD}	Supply voltage	3.0 to 3.6	V
	Static power	1.3	W
	Dynamic power with all interfaces active including external ports.(1)	3.8 at 200 Mb/s TBC	W
		1.9 at 100 Mb/s TBC	W
		0.9 at 10 Mb/s TBC	W
T_A	Ambient temperature	-55 to +125	°C

(1) If a SpW IF is not active (switched off) assume a reduction of the static and dynamic power by 5%

11.2 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are listed in Table 11-2. For a detailed list of the maximum conditions see [AD3].

Table 11-2 Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{DD}	Supply voltage range	-0.5 to +4.0	V
V_{IN}	Input voltage range	-0.5 to V_{DD}+0.5	V
I_{IN}	Input pin current		
	Signal pin	-10 to +10	mA
	Power pin	-60 to +60	mA
	Lead temperature (soldering 10 sec)	+300	°C
T_s	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	175	°C

2. USER APPLICATIONS

The SpW-10X SpaceWire router device may be used in several different ways as described in the following sub-sections.

Note: SpW-10X is pronounced "*SpaceWire Ten X*". This name derives from the abbreviation for SpaceWire (SpW), the fact that the router has eight SpaceWire ports and two external ports giving ten ports in total, and the used of "X" to represent a cross-bar switch.

2.1 STAND-ALONE ROUTER

The SpaceWire Router may be used as a stand-alone router with up to eight SpaceWire links connected to it. Configuration of the routing tables etc. may be done by sending SpaceWire packets containing configuration commands to the router.

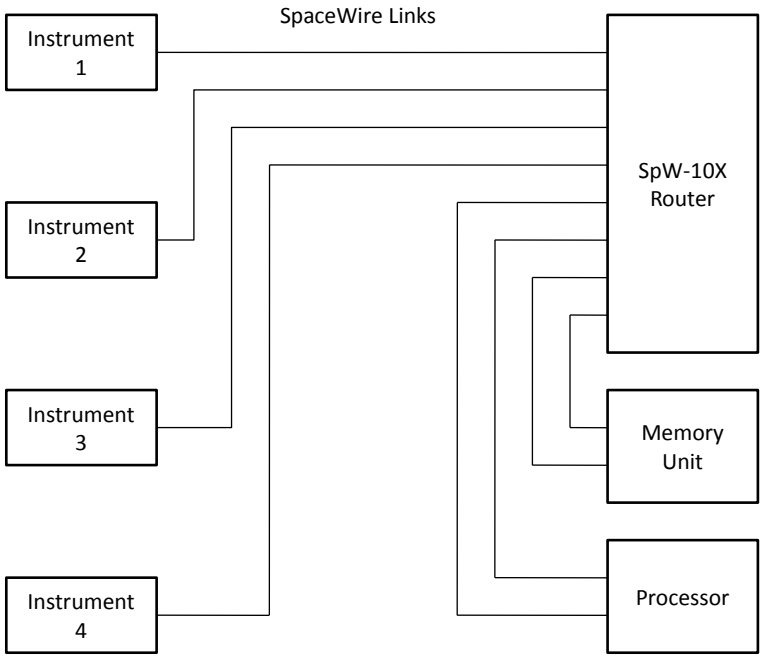


Figure 2-1 Stand-Alone Router

In Figure 2-1 an example of use of the SpW-10X device as a stand-alone router is illustrated. There are four instruments connected to the SpW-10X device along with a memory unit and processor. The processor can communicate with all the instruments and memory unit to control them and is also able to configure the SpW-10X device. The instruments can send data to the memory unit for storage or to the processor for immediate processing. The processor can also read data from the memory for later processing, writing the processed data back into memory. A pair of SpW-10X devices can be used to provide a redundant configuration.

2.2 NODE INTERFACE

The SpaceWire Router has two external ports which enable the device to be used as a node interface. The equipment to be connected to the SpaceWire network is attached to one or both external ports. One or more SpaceWire ports are used to provide the connection into the SpaceWire network. Unused SpaceWire ports may be disabled and their outputs tri-stated to save power. In this arrangement configuration of the routing tables and other parameters may be done by sending configuration packets from the local host via an external port or from a remote network manager via a SpaceWire port.

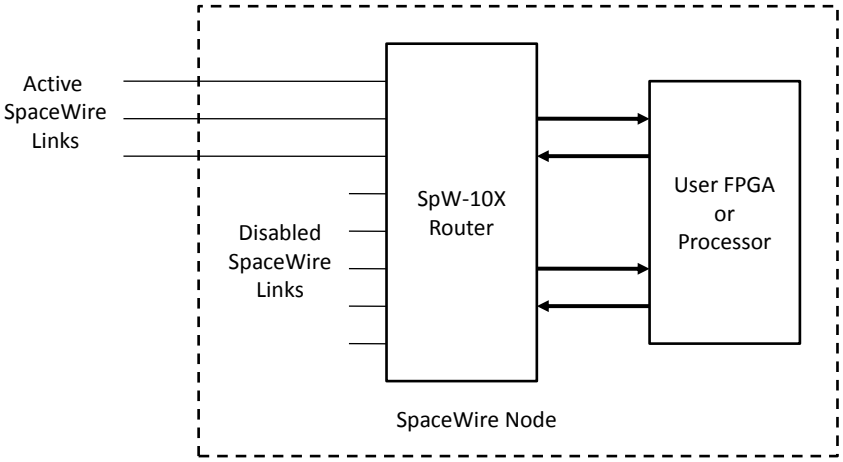


Figure 2-2 Node Interface

In Figure 2-2 a SpW-10X router is used as an interface to a user FPGA or processor, which may be part of a SpaceWire enabled instrument, control processor or other sub-system. The interface to the user FPGA or processor is via the external FIFO ports of the SpW-10X router. Only three SpaceWire links are needed for this SpaceWire node so the other five links are disabled to save power.

2.3 EMBEDDED ROUTER

The SpaceWire Router device can also be used to provide a node with an embedded router. In this case the external ports are used to provide the local connections to the node and the SpaceWire ports are used to make connections to other ports in the network. The difference between this configuration and that of section 2.2 is just a conceptual one with the Node interface configuration normally using fewer SpaceWire ports than the Embedded Router configuration.

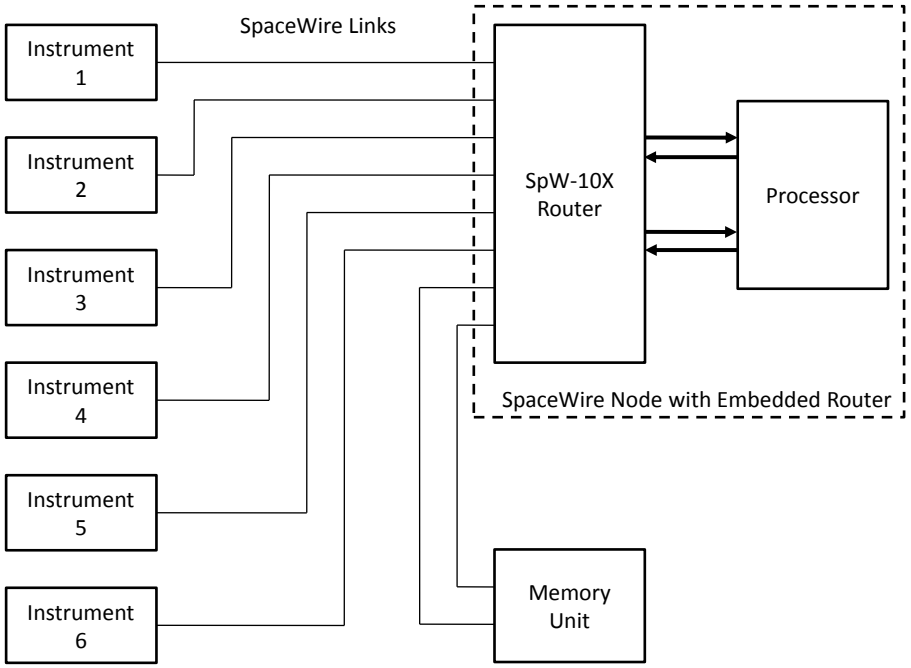


Figure 2-3 Embedded Router

In Figure 2-3 a SpaceWire system similar to that shown in Figure 2-1 is shown with the SpW-10X router embedded in a SpaceWire node along with a processor. The processor interfaces can interface to the SpW-10X router using the external FIFO ports saving some SpaceWire ports for connecting to additional instruments. For redundancy a pair of the SpaceWire nodes with embedded routers may be used.

2.4 EXPANDING THE NUMBER OF ROUTER PORTS

If a routing switch with a larger number of SpaceWire (or external) ports is required then this can be accomplished by joining together two or more routers using some of the SpaceWire links. For example using two SpaceWire links to join together two router devices would create an effective router with twelve SpaceWire ports and four external ports. Note, however, that an extra path addressing byte is needed to route packets between the two routers and that there is additional routing delay.

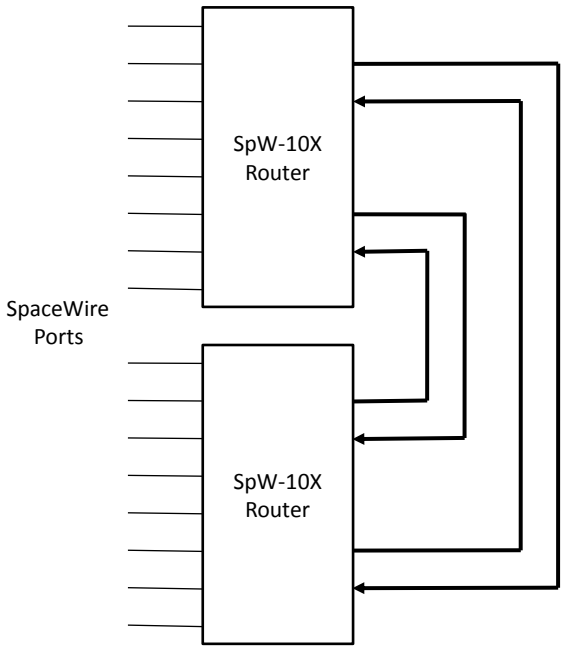


Figure 2-4 Expanding the number of SpaceWire Ports (1)

Figure 2-4 shows a pair of SpW-10X routers connected together using the external FIFO ports to provide a 16 port router. A small amount of external logic is required to connect the external FIFO ports in this way. Note that the bandwidth between the two SpW-10X devices is limited by the two external FIFO ports used to interconnect them. Each FIFO port can handle one SpaceWire packet at a time in each direction.

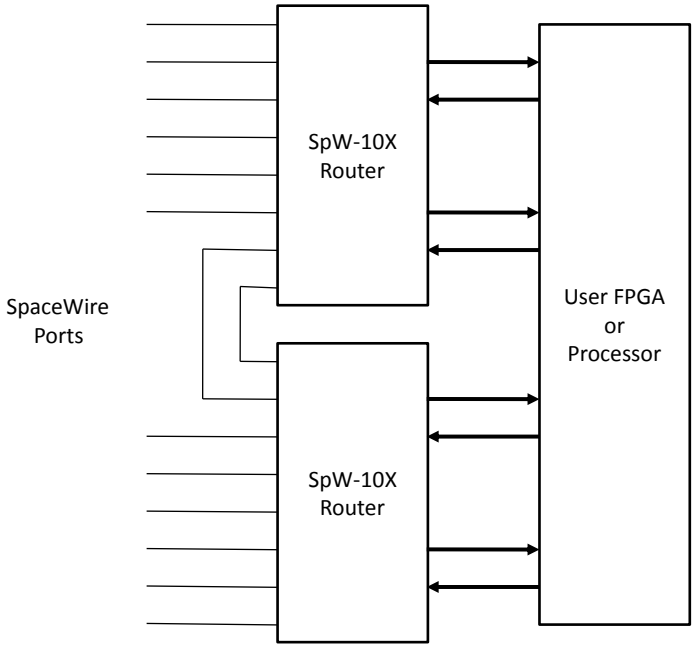


Figure 2-5 Expanding the number of SpaceWire Ports (2)

Figure 2-5 shows two SpW-10X router devices interconnected using two of the SpaceWire ports on each router. This leaves twelve SpaceWire ports for connection to other SpaceWire nodes. The External FIFO ports of each router are used to connect to user logic in an FPGA or to a processing device.

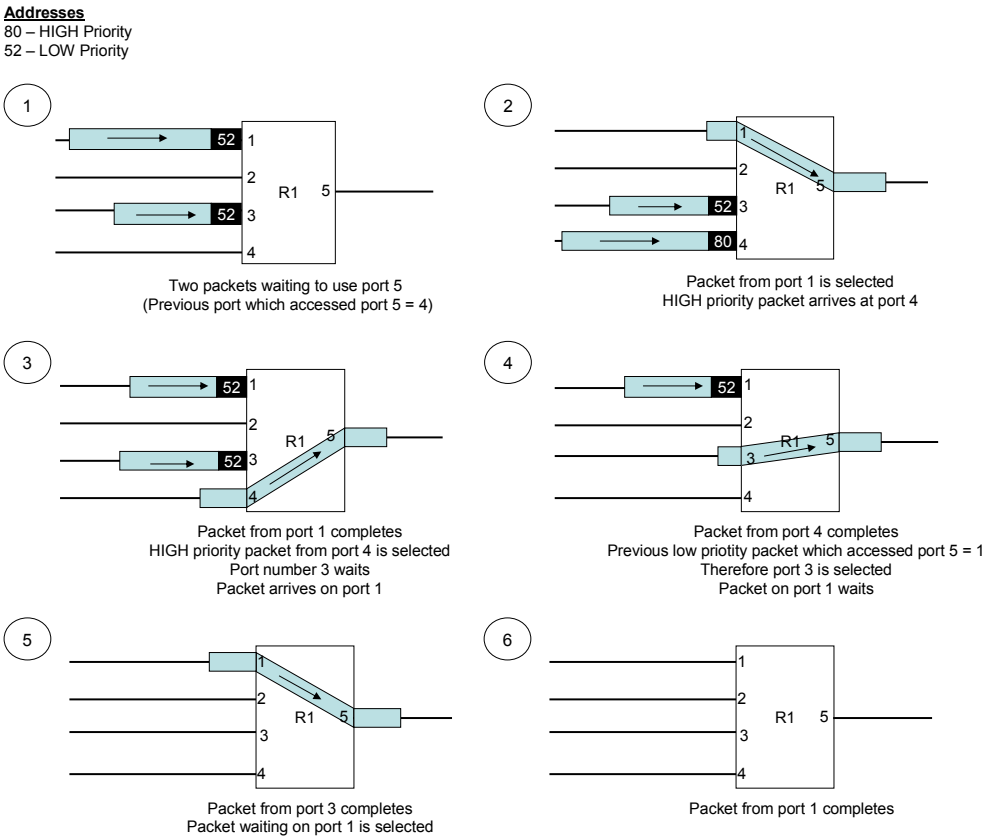


Figure 8-7 Arbitration of two packets with different priority (2)

8.3.5 Packet Blocking

The Time-Out Enable bit (bit 0) of the router control register enables the watchdog timers on the ports. When this bit is set and the watchdog timers are enabled the router is in “Watchdog Timer” mode. When it is clear and the watchdog timers are disable then the router is in the “Blocking Allowed”mode.

In Blocking Allowed mode packets wait indefinitely on other packets to complete. An exception to this is when an output port that a packet is to be routed to is a SpaceWire port and that port is not started. In this case the packet waits as long as the timeout period and is then discarded if the output port has not started. If group adaptive routing is being used and at least one of the destination ports is running then the packet will wait indefinitely for that output port to become free or another one in the group to start.

In Watchdog Timer mode watchdog timers on the ports are used to clear packets from the network if they become blocked, either while being routed or while waiting on a port which is not granted to any other port. The watchdog timers are restarted every time a data character is transferred. They are stopped after an EOP and started again on the first data character of a packet. In this way the time to transfer a complete packet is not checked but instead the watchdog timers check if a packet has blocked (i.e. no data transfers).

A blocked packet is spilt by terminating the packet at the router output port with an EEP and spilling the remainder of the packet to be transmitted up to and including the EOP at the router input port. If the router output port is blocked (full) and cannot accept data then the EEP is added after the port is unblocked.

WARNING

Blocking Allowed mode is not recommended and should be used with caution.

When Blocking Allowed mode is used (Watchdog timers disabled) then it is important that provision is made for a network manager to detect blocking situations and to reset the nodes or routers causing the problem.

The various ways in which an input port can become blocked and the resulting actions taken by the router are considered in the following sub-sections:

8.3.5.1 Blocked destination

In a blocked destination scenario data cannot be transmitted to the destination port because there is no more transmit credit (no more FCTs received) in a SpaceWire port or an external port output FIFO has become full. Since the destination node is blocked the packet data is left strung out across the SpaceWire network from the packet source to the blockage. In this situation the tail of the packet is distributed across multiple routers and other network paths can become blocked waiting on the original blocked packet to complete.