Current Developments and Applications Session

Introduction & Status of SpaceWire Related ESA Contracts

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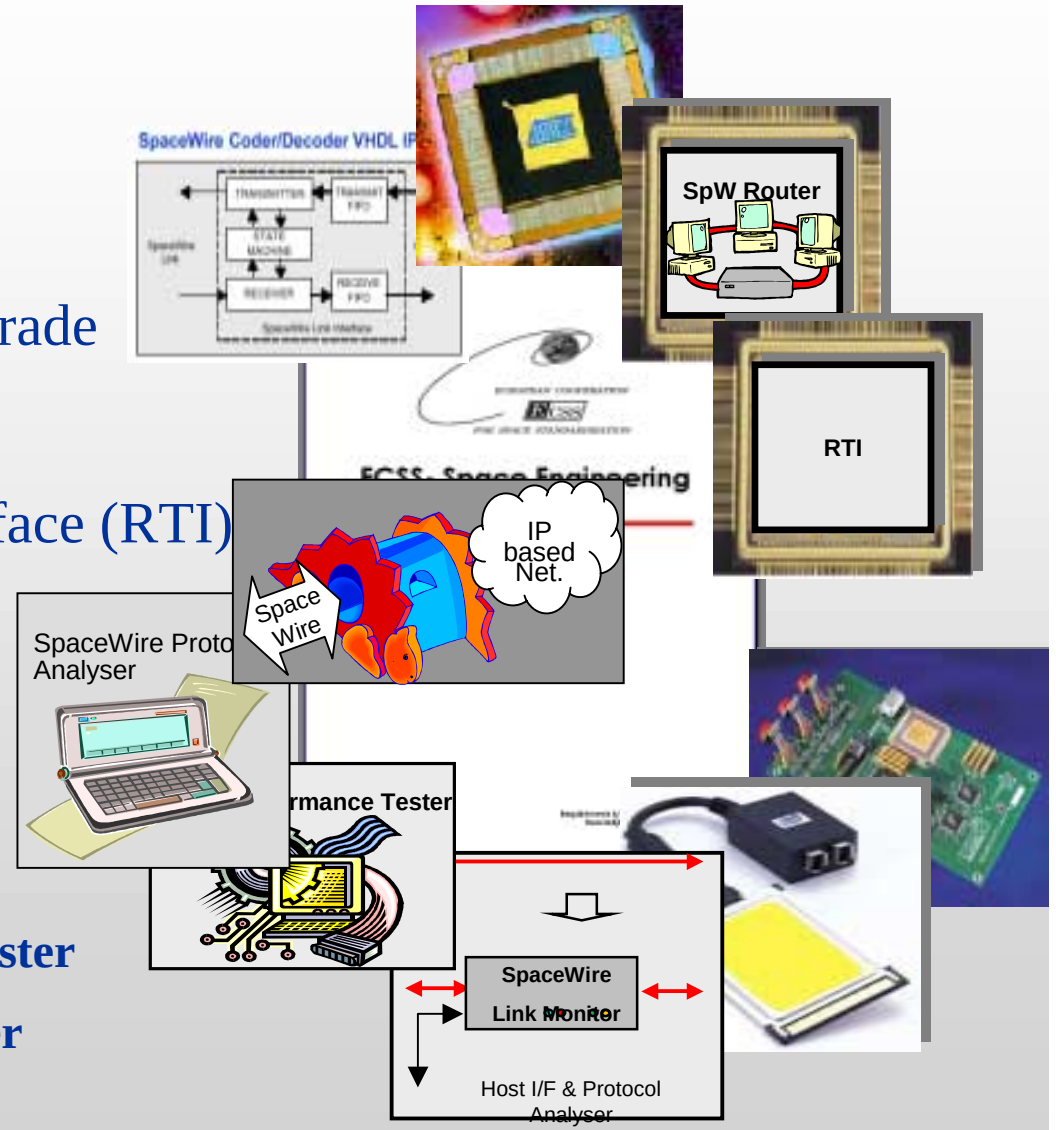
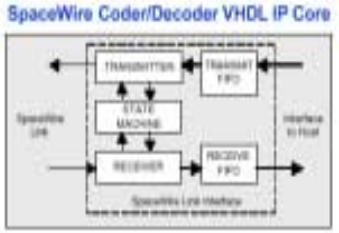
On Board Payload Data Processing Section

Outline

- SpaceWire ECSS Standard
- SpaceWire CODEC
- SMCS332 & SMCS116 Upgrade
- SpaceWire Router
- SpW Remote Terminal Interface (RTI)
- EGSE:
  - **SpaceWire PCI Card**
  - **SpaceWire PCMCIA Card**
  - **SpaceWire Link Monitor**
  - **SpaceWire Conformance Tester**
  - **SpaceWire Protocol Analyser**
  - **SpaceWire Internet Tunnel**



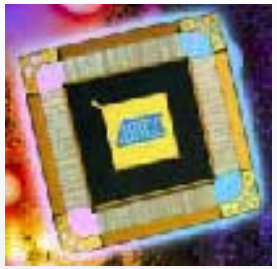
SpaceWire CODEC



New IP core, fully SpaceWire (ECSS-50-12A) compatible, distributed by ESA

- **Delivery to ESA** — **May 2003**
- **ESA Validation** — **May-Sept 2003**
- **Distribution to European entities** — **ASAP**

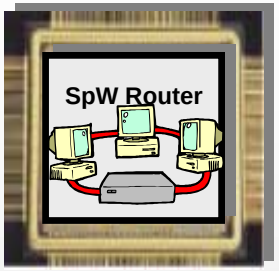
SMCS332 & SMCS116 Upgrade to SpaceWire



Second generation of SMCS332 (TSS901) and SMCS116 (T7906), fully SpaceWire compliant (ECSS-50-12A)

- **Kick-off** — **Jan 2004 (TBC)**
- **Prototype** — **Q2 2004**
- **ATMEL Standard ASIC available** — **TBD (ATMEL)**

SpaceWire Router



Development of a 8-port SpaceWire Router standard ATMEL (MH1RT) ASIC

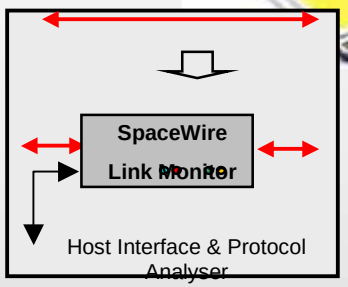
- Router FPGA — Jan 2004
- ASIC Prototype — Mar 2005
- ATMEL Standard ASIC available — TBD (ATMEL)

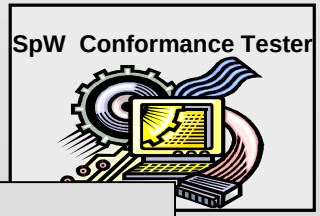
EGSEs

Next Gen. FPGA Based SpW-PCI Card, Dec 2003

SpW PCMCIA Card, Mar 2004

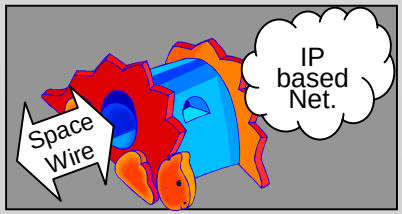
SpW Link Monitor, Dec 2003





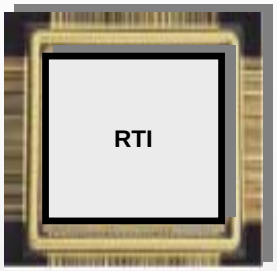
SpW Conformance Tester, Sept 2004

TopNet SpW Protocol Analyser, Dec 2004 (TBC)



SpW Internet Tunnel, Dec 2004 (TBC)

SpW RTI: a "Smart Component for Dumb Terminals"



Development of an ASIC SpW Remote Terminal Interface (RTI) for connection of nodes (with or without local intelligence)

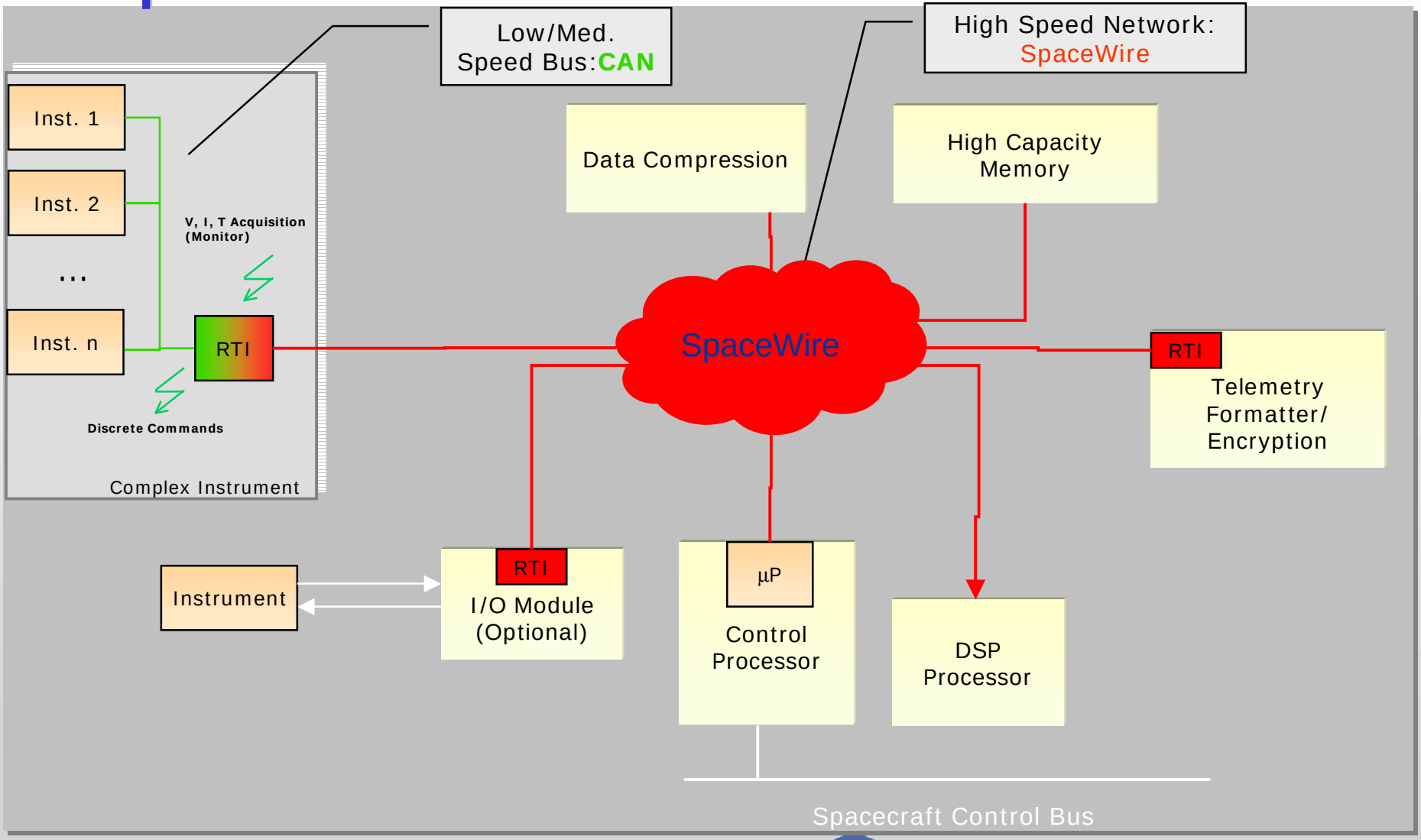
It shall be

- Configurable by link (remote control)
- Smart 'enough' to work autonomously

It shall implement

- Bridge SpaceWire-CAN

SpW RTI in OPDPS



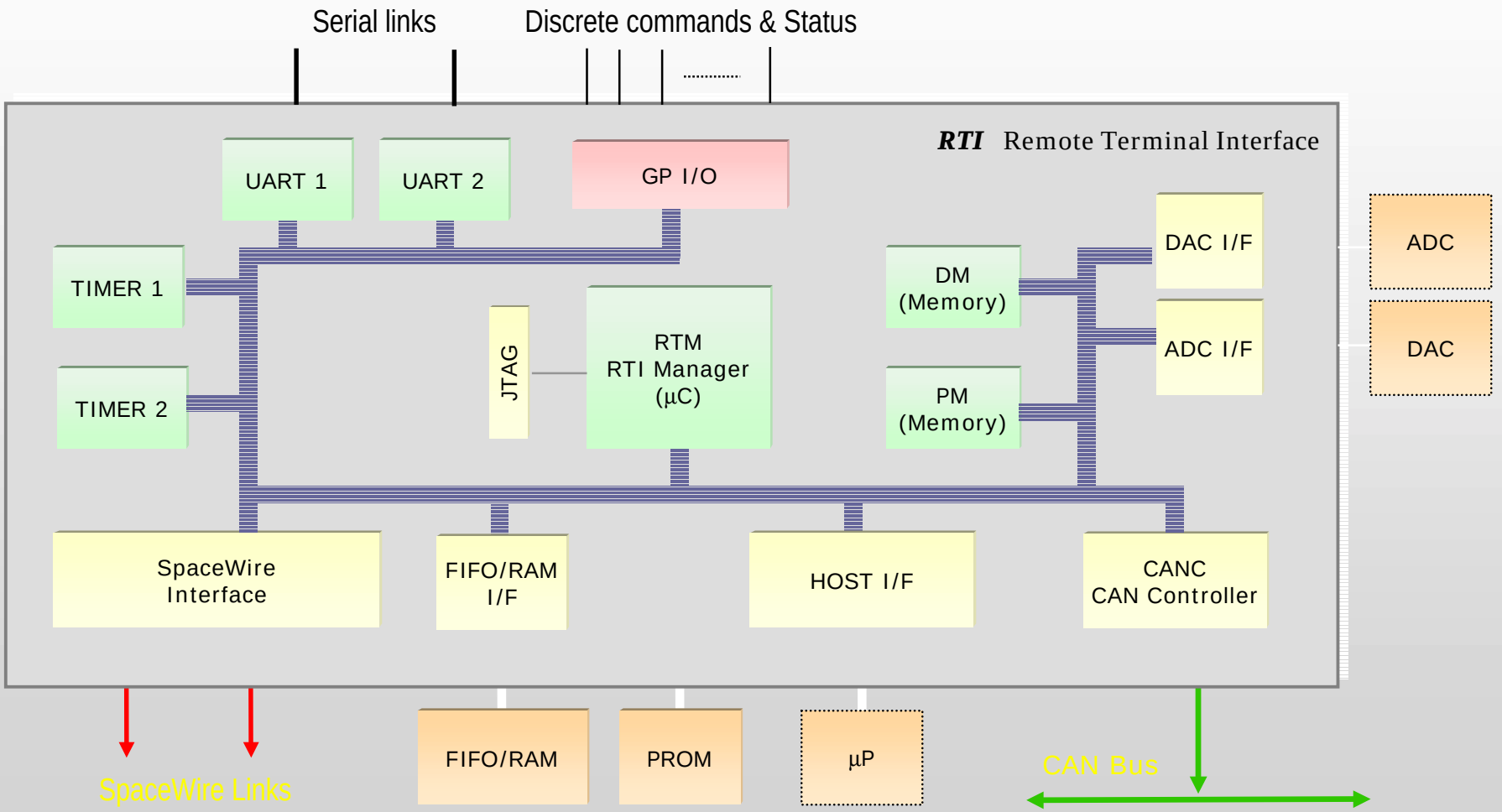
SpW RTI Requirements (1st)

- Unit configurable and controlled by link (Remote Control)
- SpaceWire I/F as high speed links
- FIFO buffering interface
- RAM buffering interface
- CAN I/F Controller (CANC)
- RTI Manager embedded µcontroller (RTM)
- GP-I/O configurable channels
  - Digital commands
  - Pulse commands
  - Digital status

SpW RTI Requirements (2nd)

- ADC Interface for analogue acquisitions
- DAC interface
- Host bus I/F
- Embedded UARTs
- Embedded user's Timers
- JTAG port for test purposes

SpW RTI Block Diagram



SpW RTI Future Expansion

- Integrated diagnostic/debugging I/F (JTAG 'like')
- Other Field/sensor Buses (1-wire®,…)
- Integrated Smart Sensors
- Wireless Links (optical and/or RF)
- ...

Budget & Planning

- Allocated Budget (excluded ASIC manufacture): 500 K€ in the frame of TopNet programme (TRP Innovative)
- ASIC Production in MPW funded by ESA
- Restrictions: non-primes (C1 category)
- ITT by fourth quarter 2003
- Duration of the contract: ≅18 months

References

I. Luca Tunesi, Philippe Armbruster, *On-board Hierarchical Network*, SPIE 2003 Barcelona (Sp), 8-10 Sept 2003

II. Philippe Armbruster, *On-board Payload Data Processing Systems*, Technical Dossier on Mapping, TOS-E-1A-DOS-1, Issue 1 Revision F, 06 Feb 2003

III. ESA/ESTEC/TOS-EDP, *SpaceWire Web Site*, http://www.estec.esa.nl/tech/spacewire/overview/

IV. EMITS: http://emits.esa.int

Thank you for Your Attention

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