The SpaceWire Router

International SpaceWire Seminar 2003

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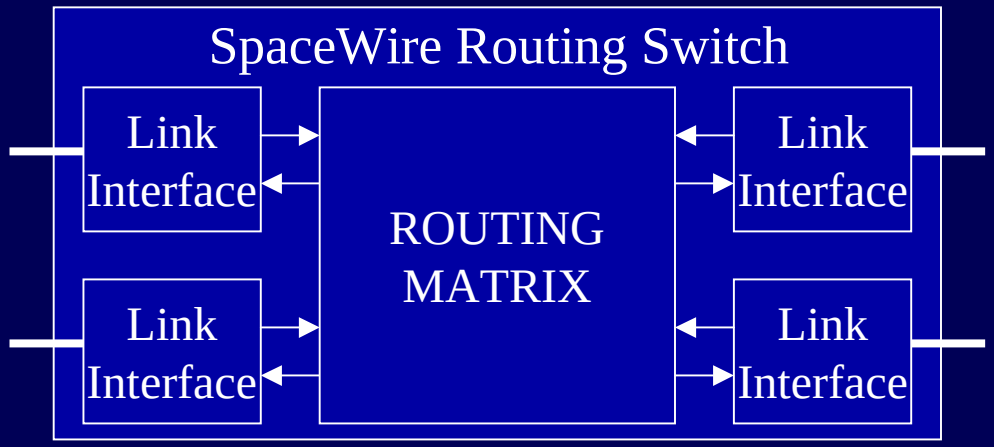
SpaceWire Packets

- Packet Format

← <DESTINATION> <CARGO> <END OF PACKET MARKER>

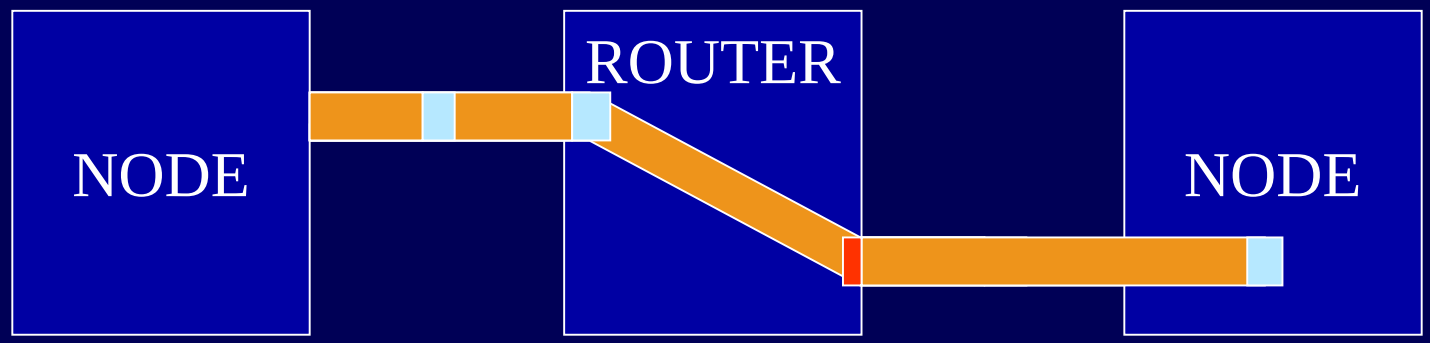
- Destination
  - represents either path to, or identity of destination node
- Cargo
  - data or message to be transferred from source to destination
- End of Packet Marker
  - indicates end of packet

SpaceWire Routing Switches



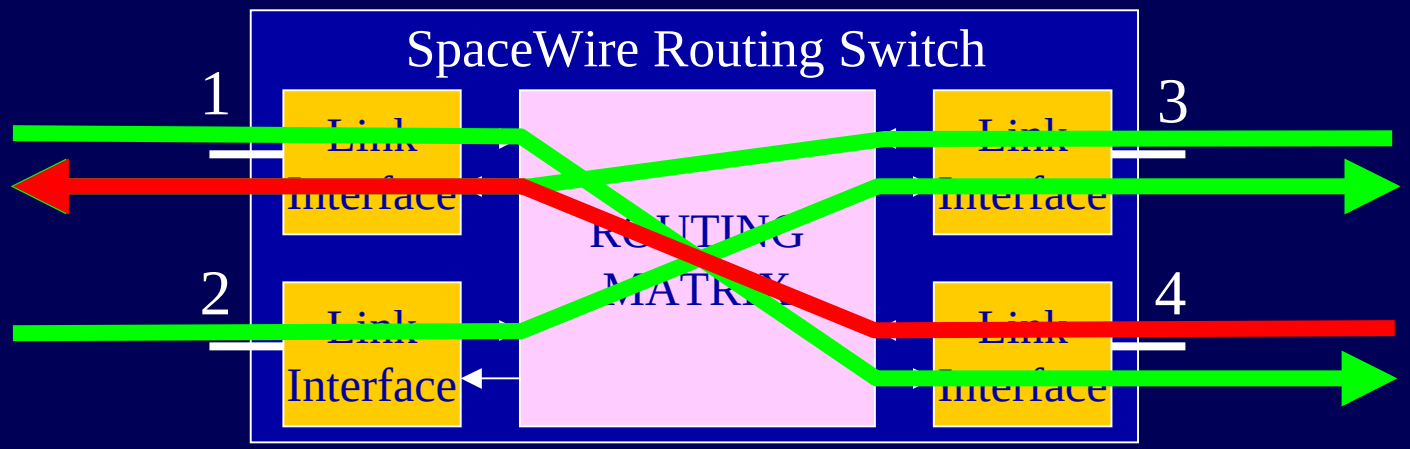
- Several link interfaces interconnected via a routing matrix.
- Wormhole routing.
- Uses leading data character of a packet as destination address / destination identifier.
- Path and Logical addressing.
- Output port arbitration.
- Priority addressing.
- Group adaptive routing.

Wormhole Routing



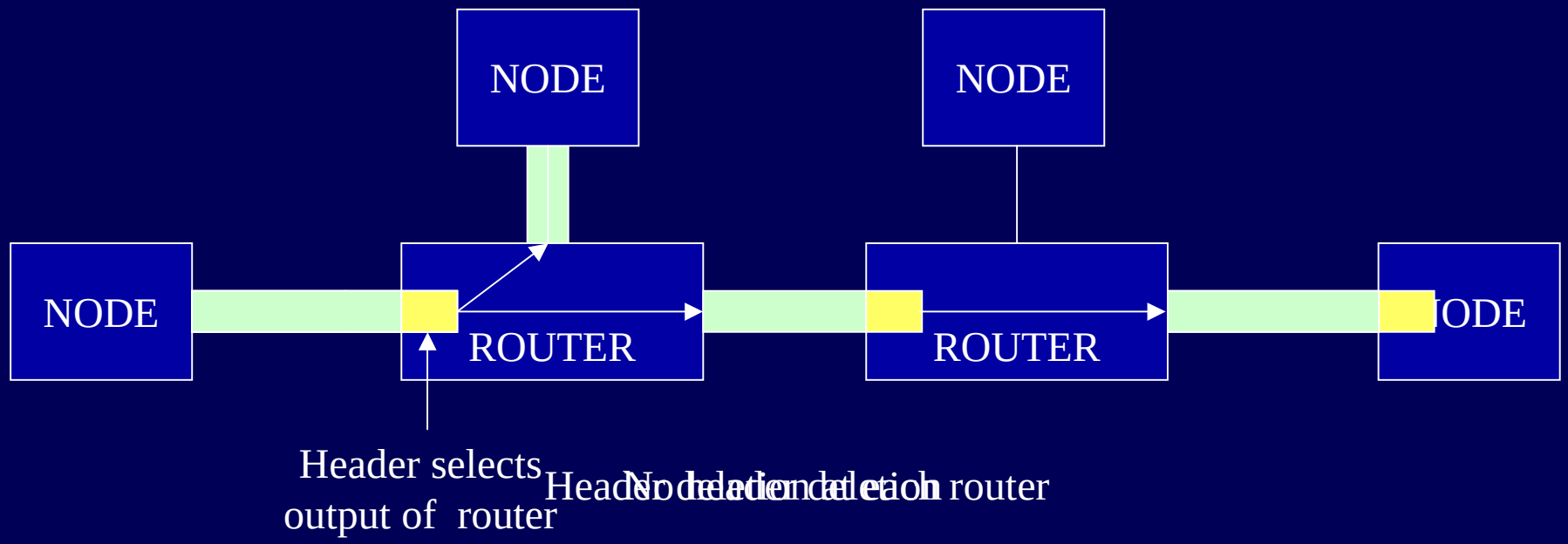
Node sends out packet
Router receives header and checks requested output port
Router connects input to output and packet flows through router
When EOP marker seen, router terminates connection
and frees output port

SpaceWire Routing Switches



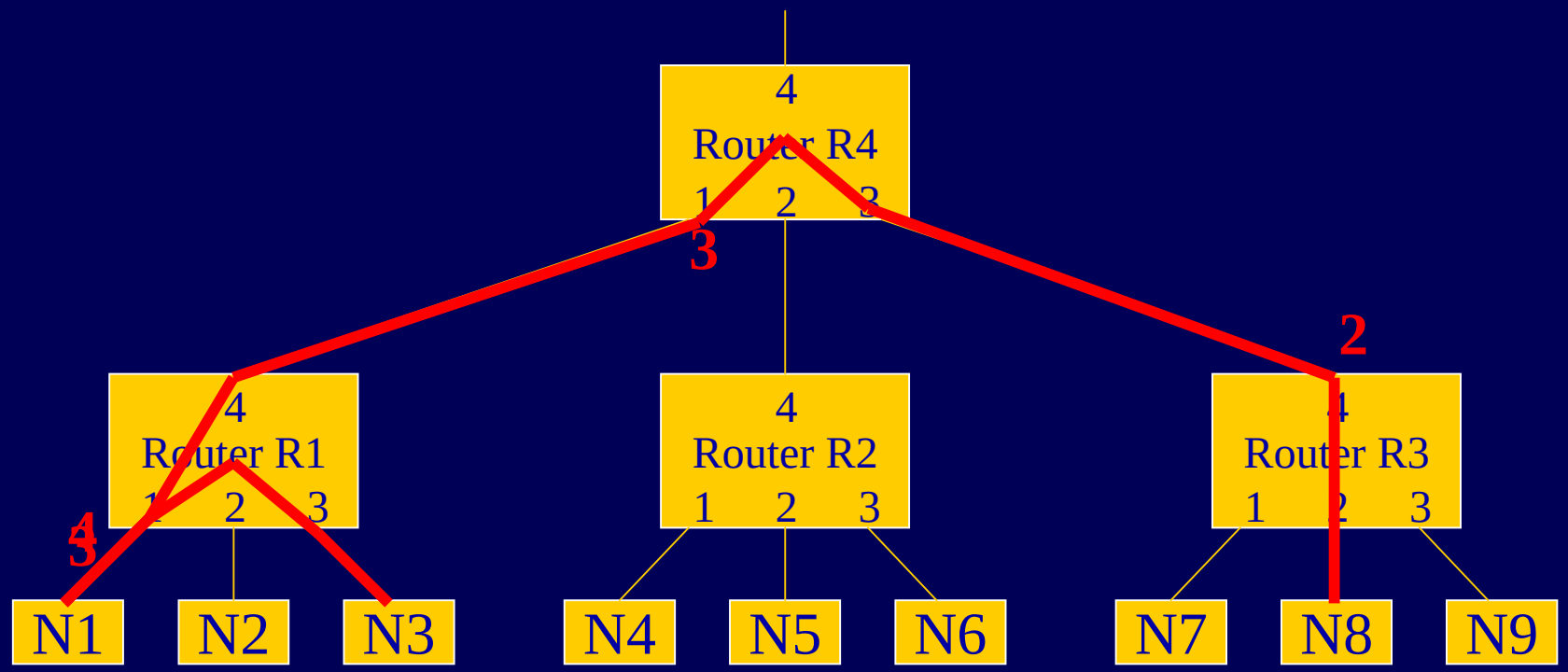
- Packet arriving at any link input
- Can be switched to any link output

Header Deletion



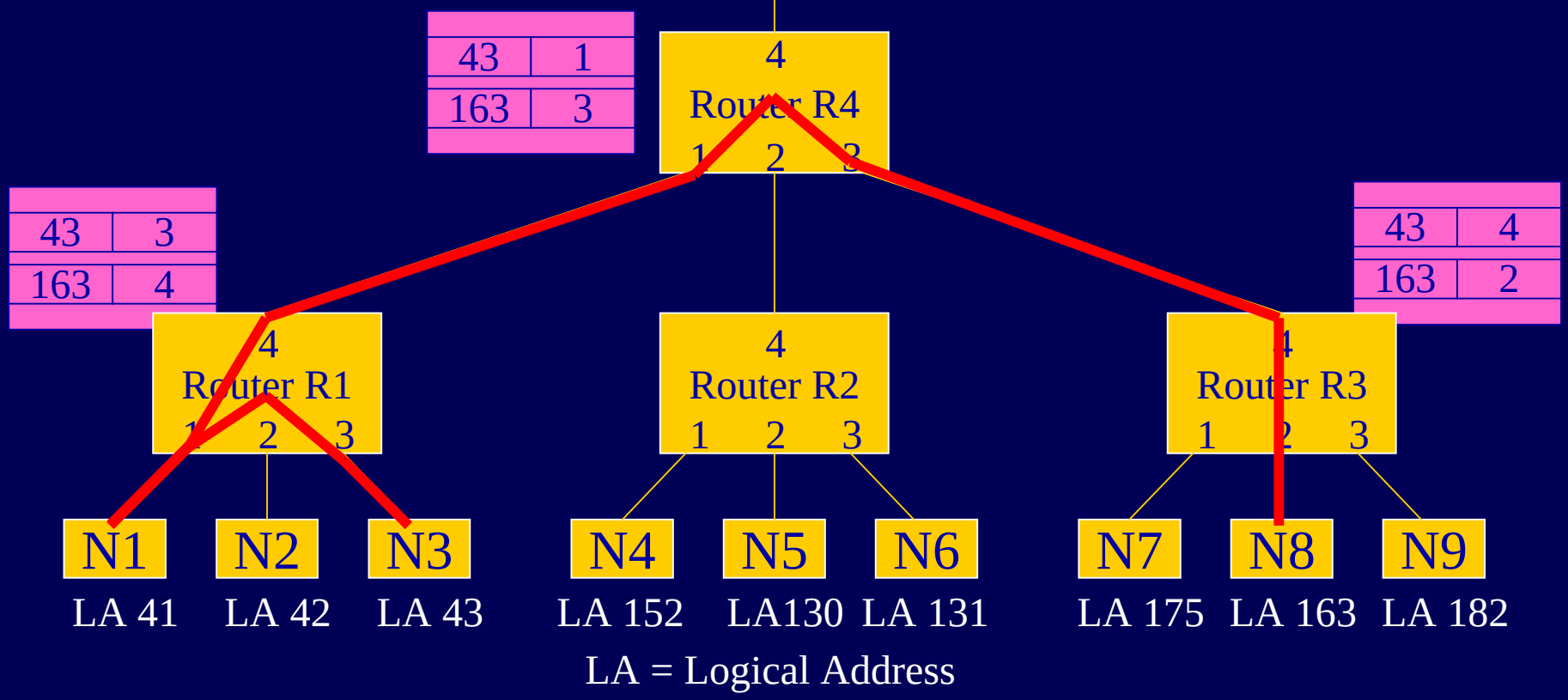
Path Addressing

- destination is specified as router output port number
- node 1 to node 3 <3><cargo><EOP>
- node 1 to node 8 <4><3><2><cargo><EOP>



Logical Addressing

- each destination has a unique logical address
- each router has a list of which port(s) to send data out for each possible destination
- node 1 to node with logical address 43 <43><cargo><EOP>
- node 1 to node with logical address 163 <163><cargo><EOP>



Routing Table

	Address	Port 0	Port 1	Port 2	Port 3	Port 4
Configuration	0	1	0	0	0	0
Path Addressing	1	0	1	0	0	0
	2	0	0	1	0	0
	…					
Logical Addressing	32	0	1	0	0	0
	33	0	0	1	0	0
	34	0	0	0	0	1
	…					
Reserved	255	0	0	0	0	0

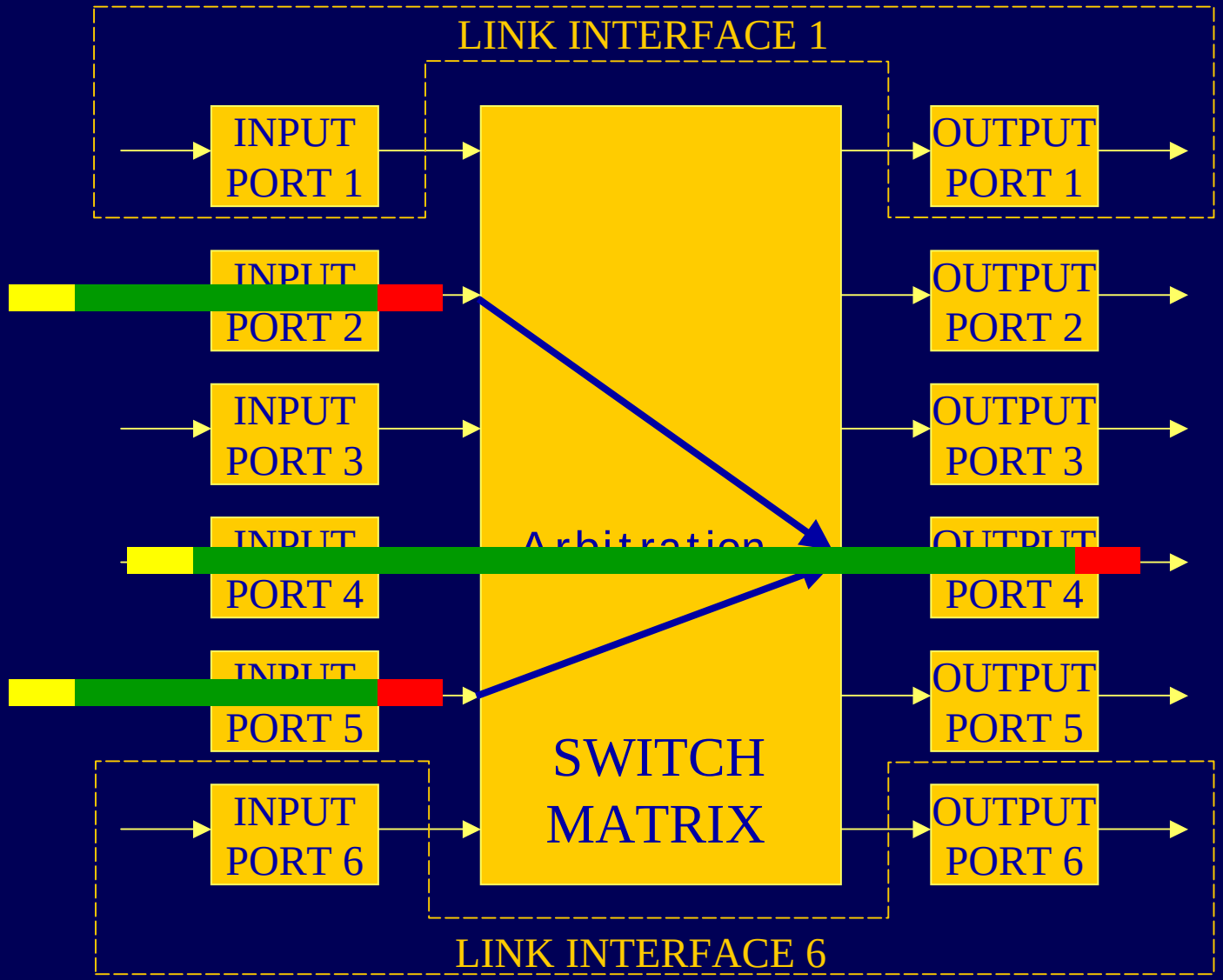
Priority

- Arbitration in Router
  - Fair arbitration
  - Priority based
- SpaceWire header contains address only
- Assign priority to logical addresses

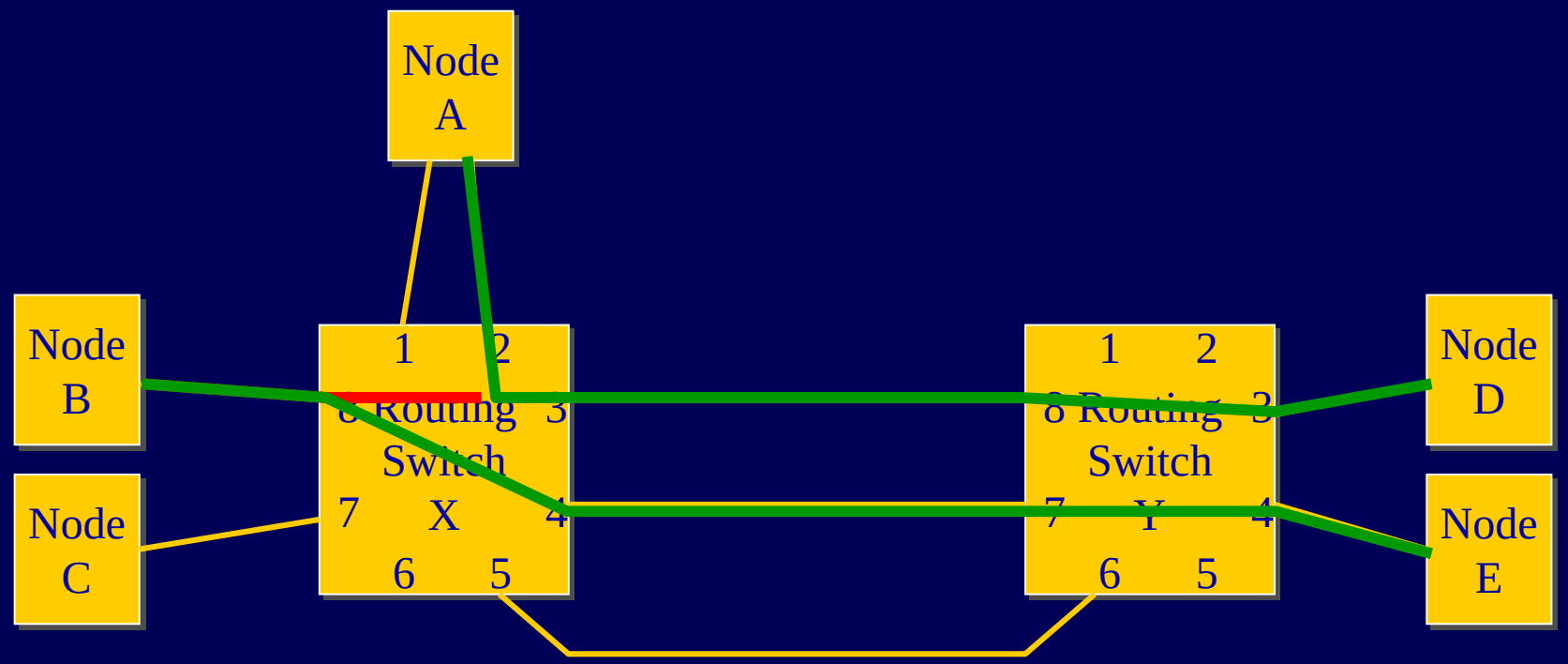
Priority

	Address	Priority	Port 0	Port 1	Port 2	Port 3	Port 4
Configuration	0	0	1	0	0	0	0
Path Addressing	1	0	0	1	0	0	0
	2	0	0	0	1	0	0
	…						
Logical Addressing	32	0	0	1	0	0	0
	33	1	0	1	0	0	0
	34	0	0	0	0	0	1
	…						
Reserved	255	0	0	0	0	0	0

Arbitration



Group Adaptive Routing



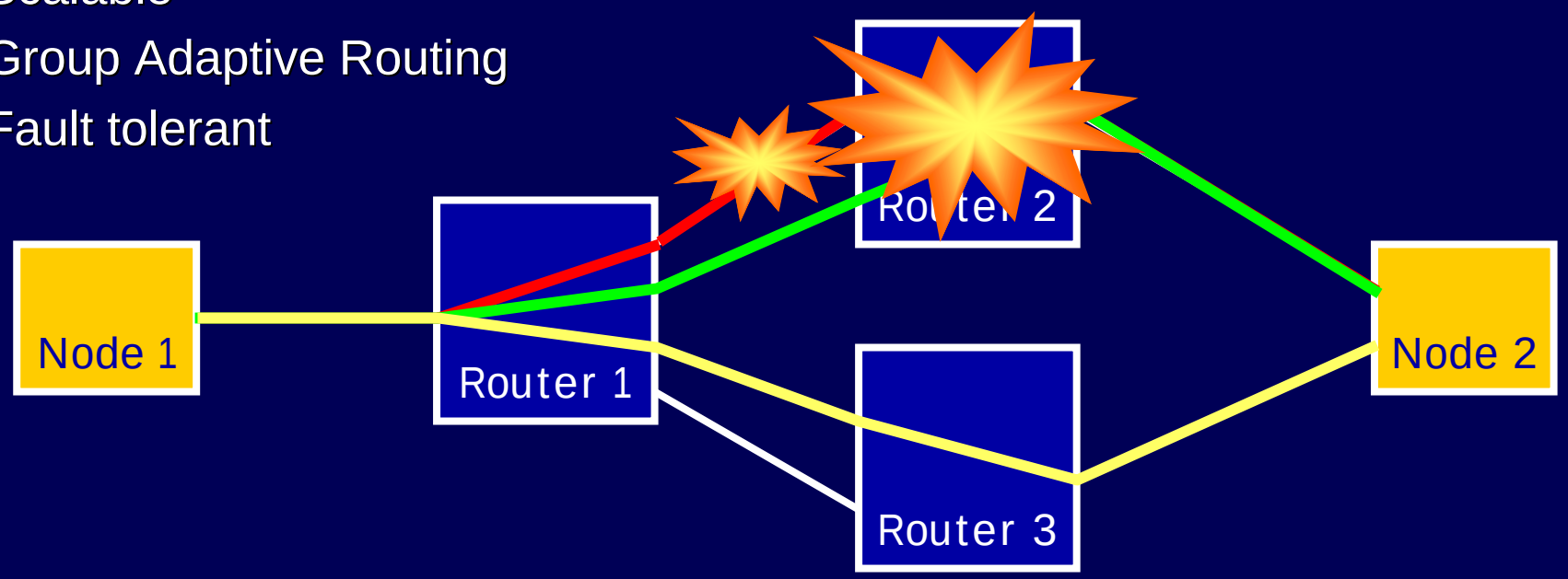
- Node B to Node E can use any of three possible links between router X and router Y
- Shares available bandwidth
- Provides support for fault tolerance

Group Adaptive Routing

	Address	Priority	Port 0	Port 1	Port 2	Port 3	Port 4
Configuration	0	0	1	0	0	0	0
Path Addressing	1	0	0	1	0	0	0
	2	0	0	0	1	0	0
	…						
Logical Addressing	32	0	0	1	1	0	0
	33	1	0	1	1	0	0
	34	0	0	0	0	1	1
	…						
Reserved	255	0	0	0	0	0	0

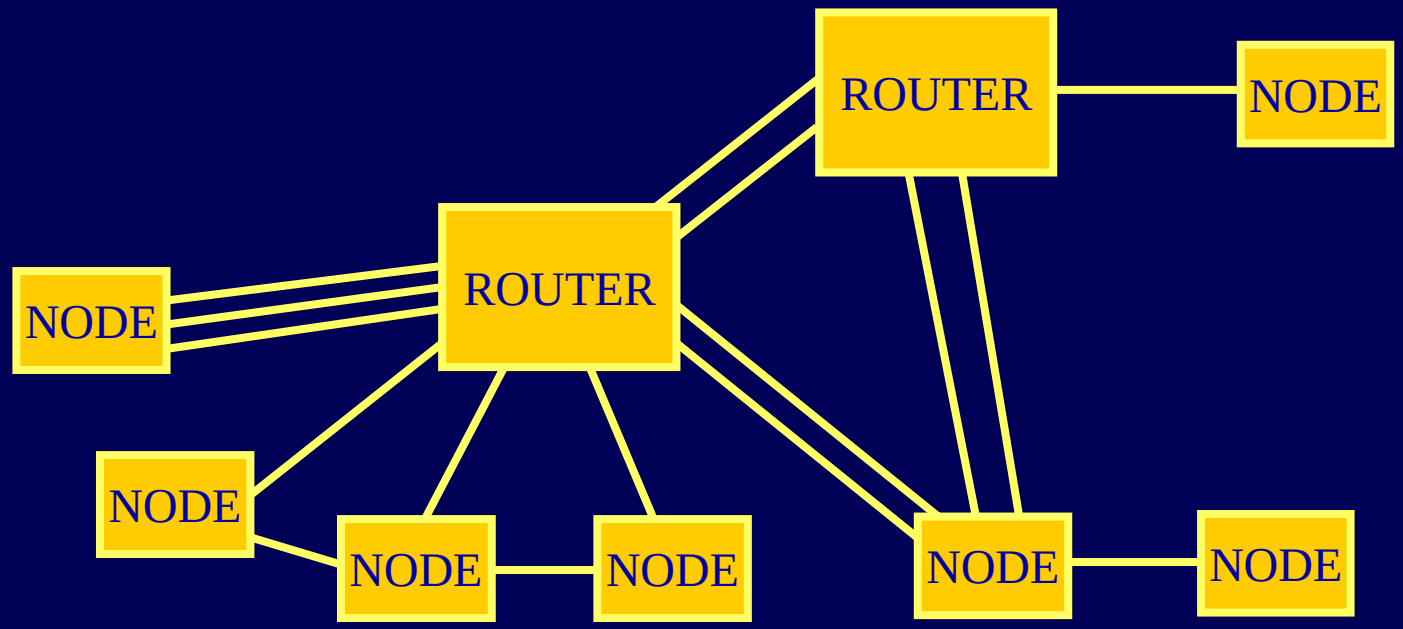
SpaceWire Features

- High speed 2-400 Mbps
- Low power <0.5 W per link interface (~5mW/Mbps @100 Mbps)
- High accuracy time distribution using time-codes
- Supports equipment compatibility and reuse
- Supports integration and test
- Scalable
- Group Adaptive Routing
- Fault tolerant



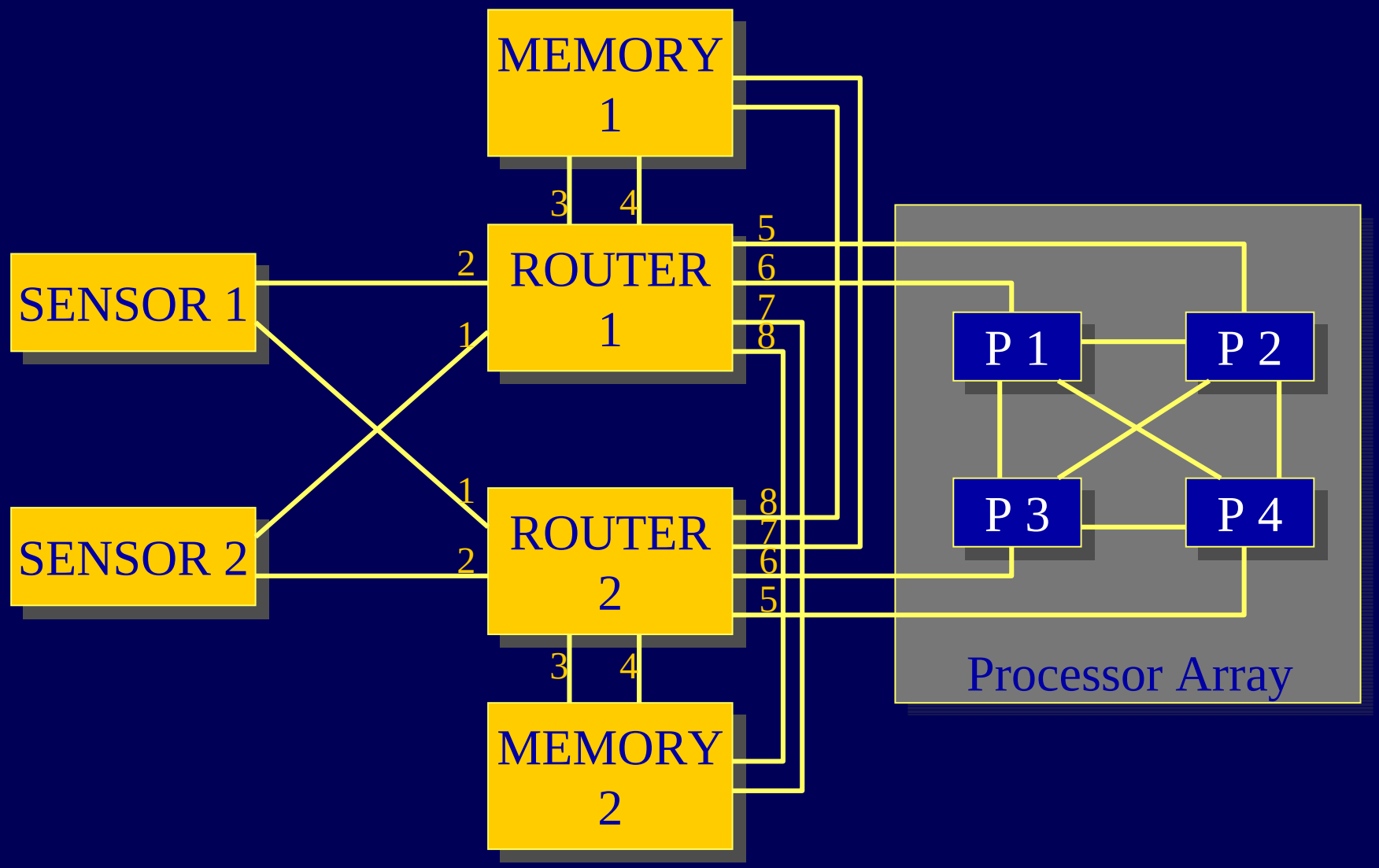
SpaceWire Network

- Two or more SpaceWire nodes
- Zero or more SpaceWire routing switches
- Interconnected with SpaceWire links

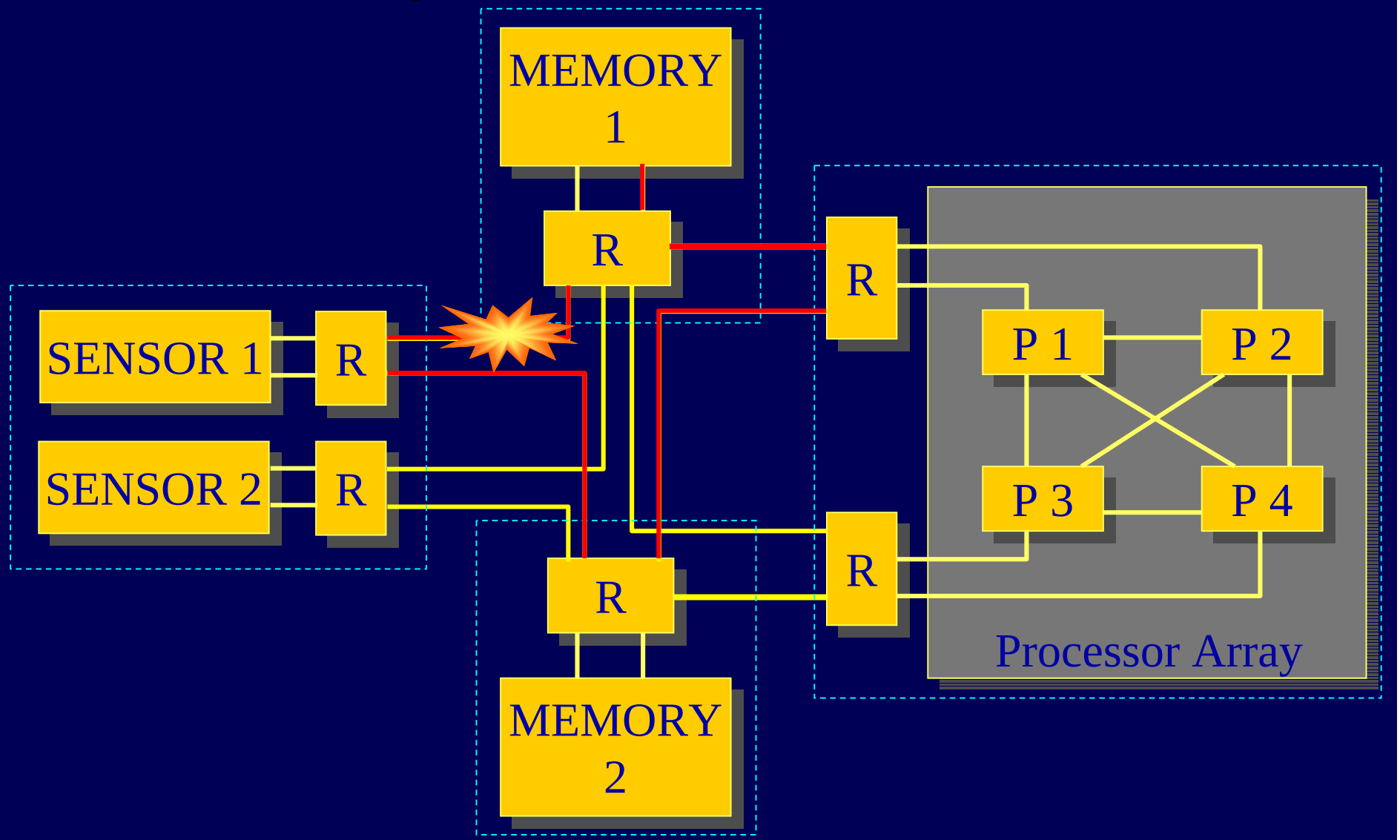


- Add bandwidth where required
- Add redundant links where required

SpaceWire Network

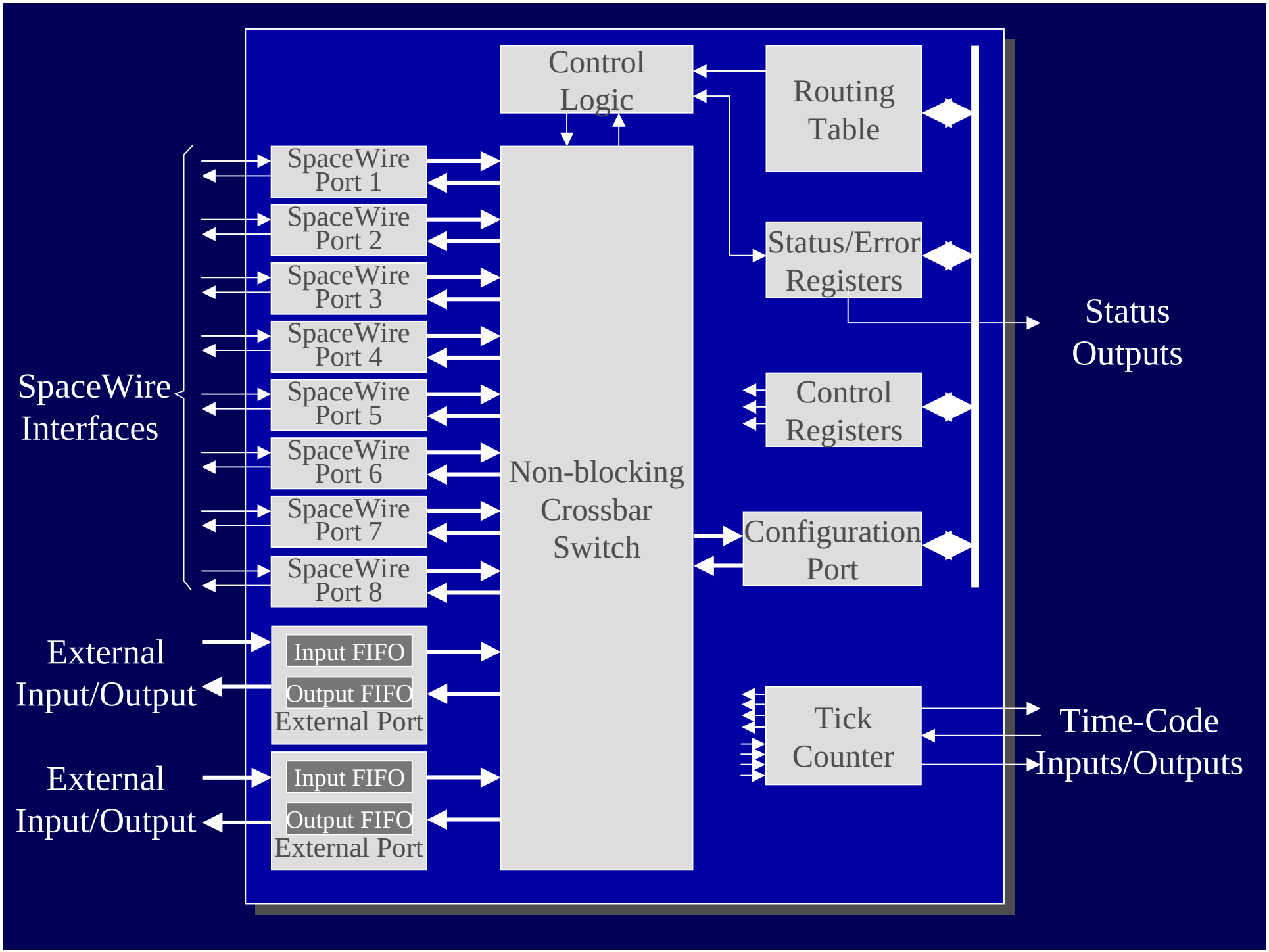


SpaceWire Network



SpaceWire Router ASIC

- Features
  - Fully SpaceWire compliant
  - Eight SpaceWire ports
  - Two External ports
  - Internal configuration port
    - Accessible through SpaceWire or External ports
    - Logical address routing table
    - Control registers
    - Status registers
  - Time-code interface
    - Receiving time-codes
    - Generating time-codes
  - External pins for status/error monitoring


Control Logic
Routing Table
SpaceWire Port 1
SpaceWire Port 2
SpaceWire Port 3
SpaceWire Port 4
SpaceWire Port 5
SpaceWire Port 6
SpaceWire Port 7
SpaceWire Port 8
Status/Error Registers
Status Outputs
SpaceWire Interfaces
Control Registers
Non-blocking Crossbar Switch
Configuration Port
External Input/Output
Input FIFO
Output FIFO
External Port
Tick Counter
Time-Code Inputs/Outputs
External Input/Output
Input FIFO
Output FIFO
External Port

Router ASIC Performance

- ASIC
  - Implementation in Atmel MH1RT gate array
  - Max gate count 519 kgates (typical)
  - 0.35 µm CMOS process
- Radiation tolerance
  - Up to 300 krad
  - SEU free cells to 100 MeV
  - Used for all critical memory cells
  - Latch-up immunity to 100 Mev
- Performance
  - SpaceWire interface baud-rate 200 Mbits/s
  - LVDS drivers/receivers integrated on-chip
- Power
  - 4 W power with all links at maximum data rate
  - Single 3.3 V supply voltage
- Package
  - 196 pin ceramic Quad Flat Pack 25 mil pin spacing

Router ASIC Schedule

- Router project started in Jan 2002
  - Router requirements
- Router contract started Sept 2002
  - CODEC designed
  - Router designed
  - FPGA implementation
  - Revised FPGA moving towards ASIC just completed
- Validation to take place from January to April 2004
  - Finalise design of router
- ASIC to be delivered in December 2004
  - Final router validation
- Router project to finish in March 2005