Procurement of
ESA-UoD SpaceWire CODEC
VHDL IP Core

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PROCUREMENT of ESA VHDL IP CORES

http://www.estec.esa.nl/wsmwww/core/corepage.html

Synthesizable IP-Cores Available from ESA

The contents of this page is related to building blocks, mostly in VHDL language, for microelectronics developed in the frame of European Space Agency (ESA) activities, ranging from in-house developments to contractor work and from simple Field Programmable Logic Arrays (FPGA) to complex System-On-a-Chip (SOC) devices.

These cores can be licensed from ESA with certain restrictions. Please read the licensing conditions.

The following ESA cores are currently available or planned.

As the area depends on multiple factors (configuration of the IP, synthesis constraints etc.), area figures given in the table are indicative only.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Status/Notes</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>EV132</td>
<td>The EV132 is a 32-bit VME interface circuit designed to interface the EBC12 processor chip to the VME bus. The EV132 fully adheres to the IEEE 1014-1987 VMEbus standard, and is compatible with the commercial VMEbus specification. EV132 can act as a system controller and provides both master and slave VMEbus. It has been implemented as a synthesizable VHDL model.</td>
<td>available</td>
<td></td>
</tr>
<tr>
<td>OSID</td>
<td>The OSID Unaugmented Code (OC) synthesizable VHDL core provides basic time keeping functions such as Elapsed Time counter according to the OSID Unaugmented Code specification. It provides accurate time keeping.</td>
<td>available</td>
<td>CTM Area on Xilinx Vertex E</td>
</tr>
</tbody>
</table>
General procedures: IP request, licence conditions

http://www.estec.esa.nl/wsmwww/core/licensing.html
General ESA IP Core Licence conditions

http://www.estec.esa.nl/wsmwww/core/ipcore_licence_template_external.pdf

To whom:

- Non-exclusive
- Non-transferable (except explicitly agreed, i.e. sub-contractors)
- Within ESA member/participant states territory

For what:

- HDL modelling, HW manufacturing
- R&D and/or commercial
- Peaceful applications (in accordance with United Nations)
SpaceWire-specific ESA Licence conditions

SGS-Thomson Microelectronics patent on part of the IEEE1355 standard used also in SpaceWire (Data-Strobe serial interface):

EP 0 458 648 A3

“Communication interface for serial transmission of variable length data tokens”


ESA is currently discussing with STM how to proceed to facilitate ESA distribution of this IP Core without infringing any STM patented rights.
SpaceWire-specific ESA Licence conditions

A special disclaimer clause in the general ESA IP Core licence might be included to:

1- Inform IP licensees about STM patent existence
2- Advise IP licensees to obtain a license from STM in case of:
   - non research/experimental use of products using the IP
   - commercial use of products that use the IP

Precise text of disclaimer is currently being discussed between ESA and STM
SpaceWire-UoD specific ESA Licence conditions

Only to be used for ESA activities and projects
(as agreed in ESA contract 15803/01/NL/JA)
PROCUREMENT of ESA SpW IP Core: the steps

1- Consult ESA IP-Cores website (http://www.estec.esa.nl/wsmwww/core/corepage.html) to:
   1.1 learn details on IP availability
   1.2 download technical documentation (IP user’s manuals, etc)
   1.3 evaluate acceptance of ESA licence conditions
   1.3 learn what info has to be sent and to whom in ESA to place a formal IP request

2- Send all requested info (company, end users, application, technology, etc) to ESA/ESTEC/IMT-CTE (TOS-EDM Contracts Section)

3- If all conditions are met, ESTEC will send to the prospect licensee a licence document tailored for his case. Depending on licensee’s relation with ESA, this document will be:
   3.1 Prospect ESA contractor: contract including a licence Annex
   3.2 Current ESA contractor: CCN including licence terms
   3.3 Other: ad-hoc licence (1KEuro fees apply)

4- Upon reception at IMT-CTE of accepted licensing document (i.e. bearing licensee’s signatures), TOS-EDM will send the source VHDL code to licensee.