MCFlight™

SOC – BASED CHIPSET WITH SPACEWIRE LINKS FOR AEROSPACE APPLICATIONS

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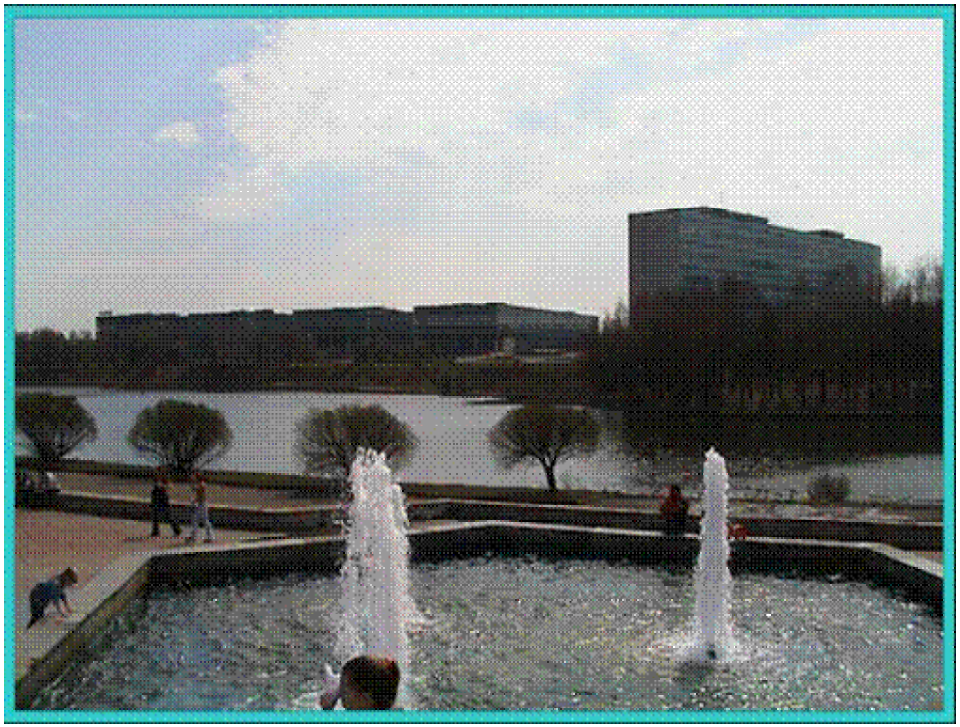
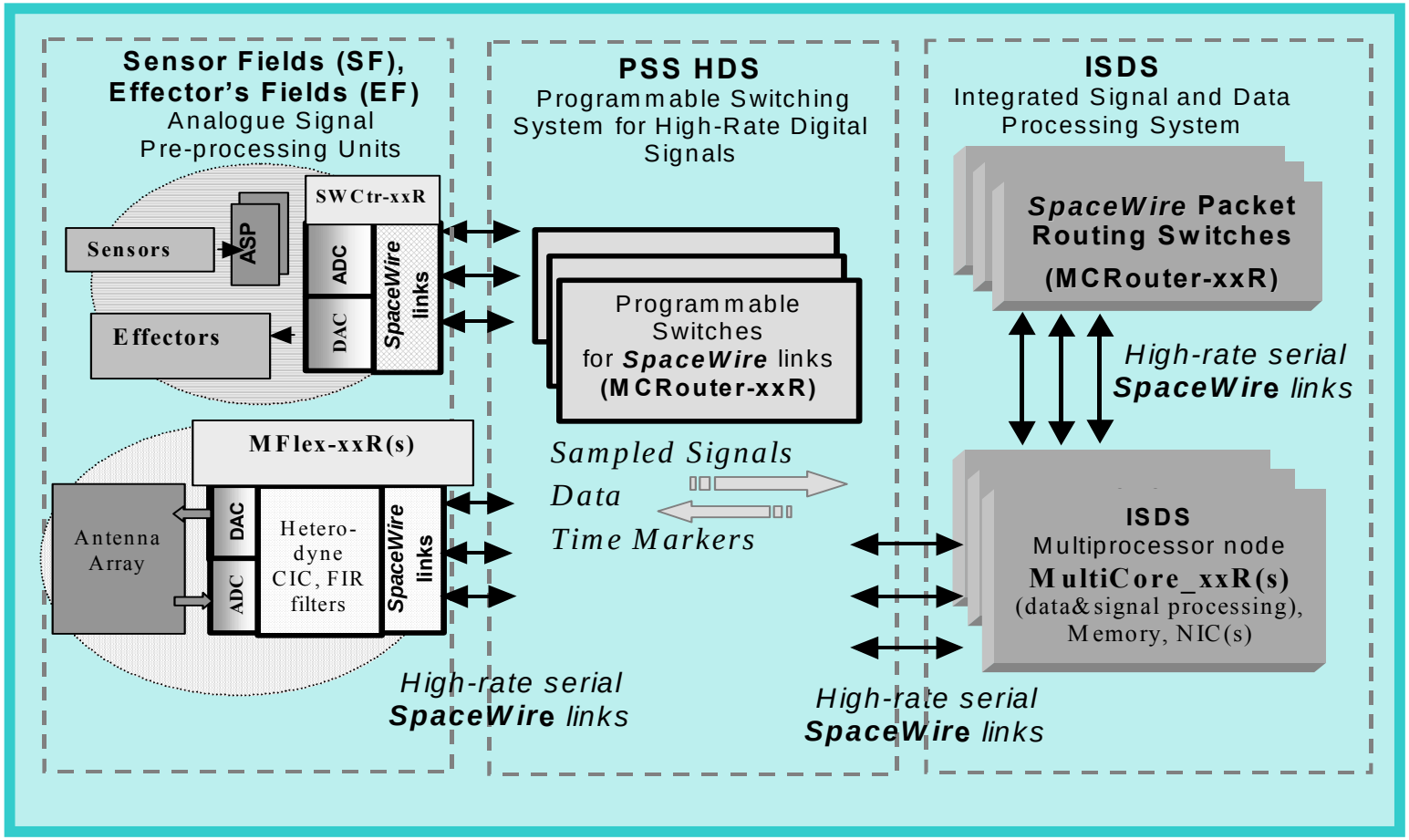
“ELVEES” R&D Microelectronics Center profile:



- was created in 1990 as a part of major in USSA space electronics corporation ELAS;
- in 1974 - the first in the USSA CMOS chip;
- more than 400 successfully developed chips;
- SOC&embedded systems& security

CONTENTS

Distributed Integrated Modular Architecture for Spacecraft On-board Systems



The MCFlight™ chipset *)

Chips type	Functional purpose
✓ MultiCore (MC - xxR™)	Dual processor (RISC&DSP cores) mooched series of scalable and flexible DSC (Digital Signal Controllers) with SpW Links , 3- 4Q2003 **)
✓ MultiFlex (MFlex-xxR™)	SDR based DDC/DUC monochip series with SpW Links and built-in ADC/DAC (in plans), 2Q2004 **)
✓ MCRouter-xxR	Multichannel (16 –channel for 1st realization) Routing switch chip with SpW, 4Q2004 **)
✓ SWCorE-xxR	Scalable and flexible high performance Serial Communications SpaceWire Controller / Remote-User-Interface ASIC with SpW Links, 3Q2004 **)

*) radiation tolerant (in plans), 0.25µ **) silicon prototyping without radiation tolerant

“MultiCorE™” Platform

Applications

SOFT

Algorithms

Software Tools

Application Software

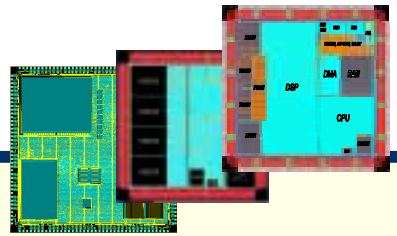
SOC DESIGN TECHNOLOGY

HARD

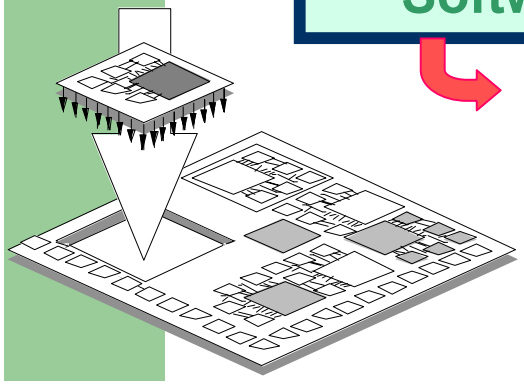
Architecture

IP-CORES LIBRARY

6-9 MONTHLY design flow



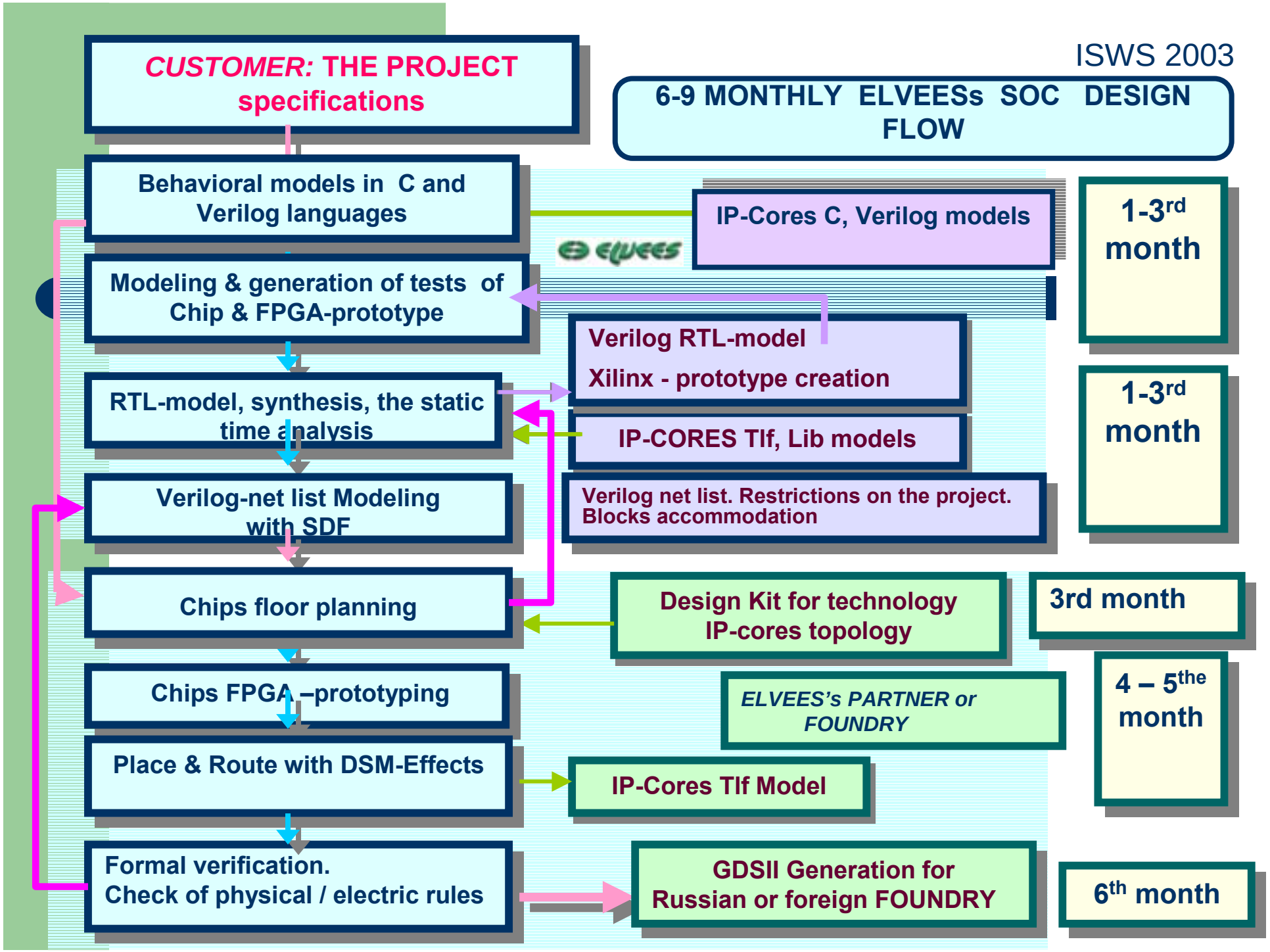
TEST Chips examples



What are the basic features of the "MultiCorE™" platform?:

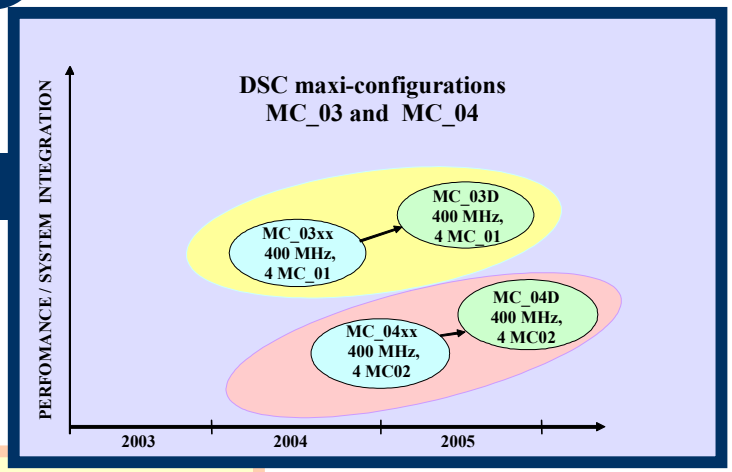
- Openness, scalability and flexibility
- 6-9 month's ELVEESs ASIC design flow for SOC integration in Chips
- Multiple processors on the chip (RISC + DSP=DSC – Digital Signal Controller)
- Improved system performance for Digital Signal Controllers (tens GOPs, GFLOPs)
- SW/HW ASIC co - verification on CAD facilities and FPGA prototyping
- Reduced Chip&System Projects development cost and time to market : 3-5 times
- Powerful Tools - MultiCorE Studio (MCStudio™)

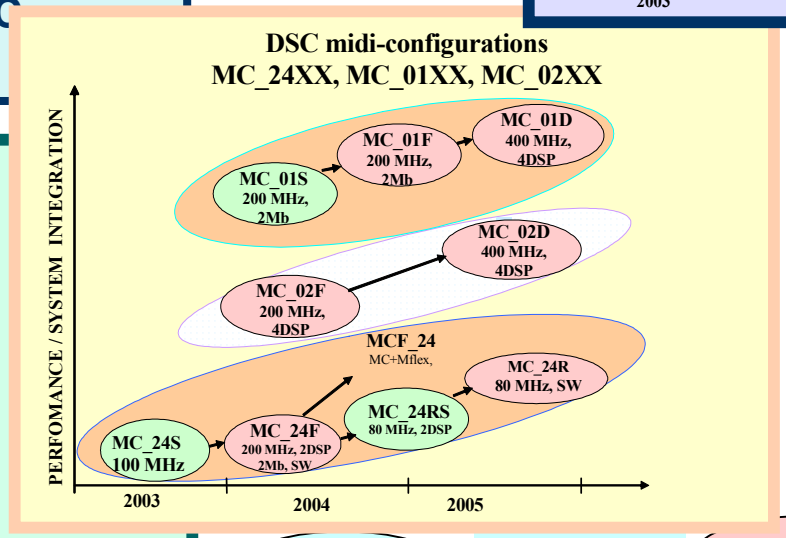
6-9 MONTHLY ELVEESs SOC DESIGN FLOW

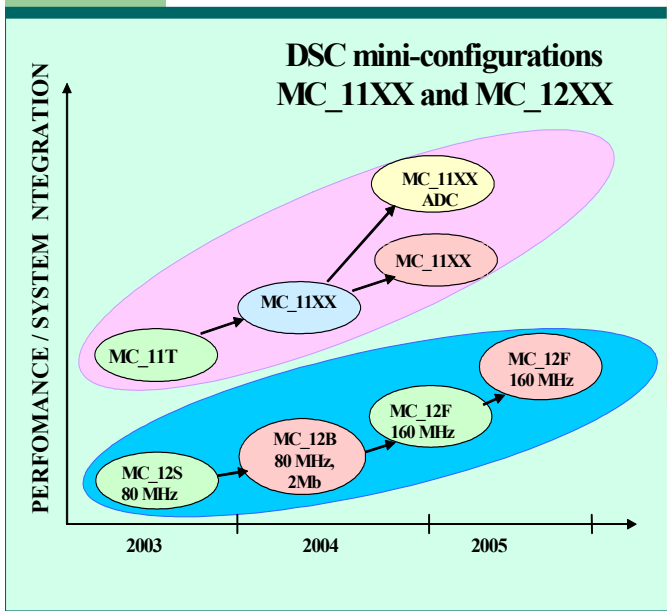


DSC MC_xx series:
MC_11/12/24/01/02/MFlex/MCF-xx… MC - xxR

- System integration (multiprocessors, SIMD/MIMD)
- Productivity on the float & fixed point
- Volume of the internal memory
- Presence built - in ADC/DAC
- special cores etc.







The project

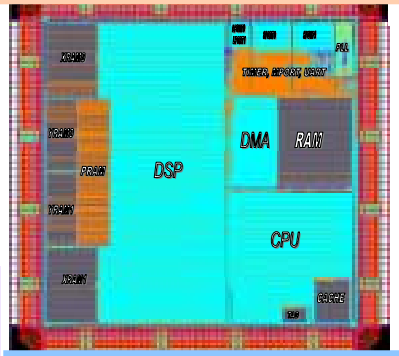
Mass production

Test chip

In plans

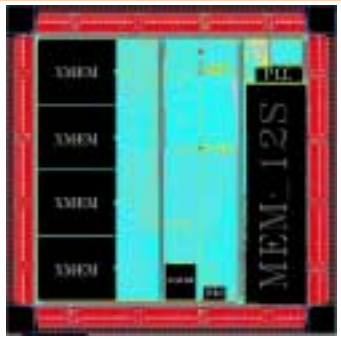
On the basis of MultiCore SoC technology "ELVEES" develops over 10 projects of modern complex multiprocessors monochips simultaneously (also MCFlight chipset with Space Wire Links). **Only in 2003 will be developed and made 3 test MultiCore chips: MC-11/12/24 (series in 1Q2004)**

MultiCore-24. 2SIMD- configurations DSC with the amplified fixed point for built in applications (Test chip – Nov. 2003)



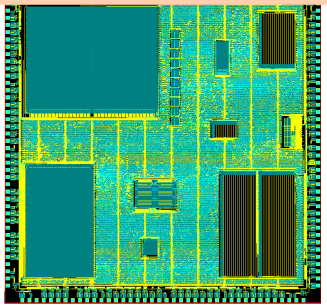
10M transistors & 0.25-mkm & 9.7*9.7 mm*mm In a series - 1Q2004.: 600MFlOPs/ 12800MOPs*1b/ 3600MOPs*8b/ 1600MOPs*16b/ 1000MOPs*32b

MultiCore-12. Mini-configurations DSC, float/fixed point for micro miniature precision embedded applications (Test chip-July 2003)



10M trans.& 0.25-mkm & 9.7*9.7 mm*mm In a series – 1Q2004.: 300MFlOPs/ 6400MOPs&1b/ 1800MOPs&8b/ 800MOPs&16b/ 500MOPs&32b

MultiCore-11T. DSC mini-configurations with the fixed point for built-in applications (test chip - December 2002)



2.5M transistors & 0. 56 -mkm & 9.6*9.6 mm*mm: 400MOPs*8b/150MOPs*16b/50MOPs*32b

“MultiCorE™” IP Cores library

- **Set of similar MIPS32 architecture ELVEES’s RISC - cores**
(with MAC, without TLB, with FPU, rad hard - RISCorE_xxR™, etceteras)

- **Set of 12 float/fixed SIMD scalable ELVEES’s DSP – cores**
(ELcore_11™/ELcore_12™/ ELcore_13™/ ELcore_14™ , etceteras)

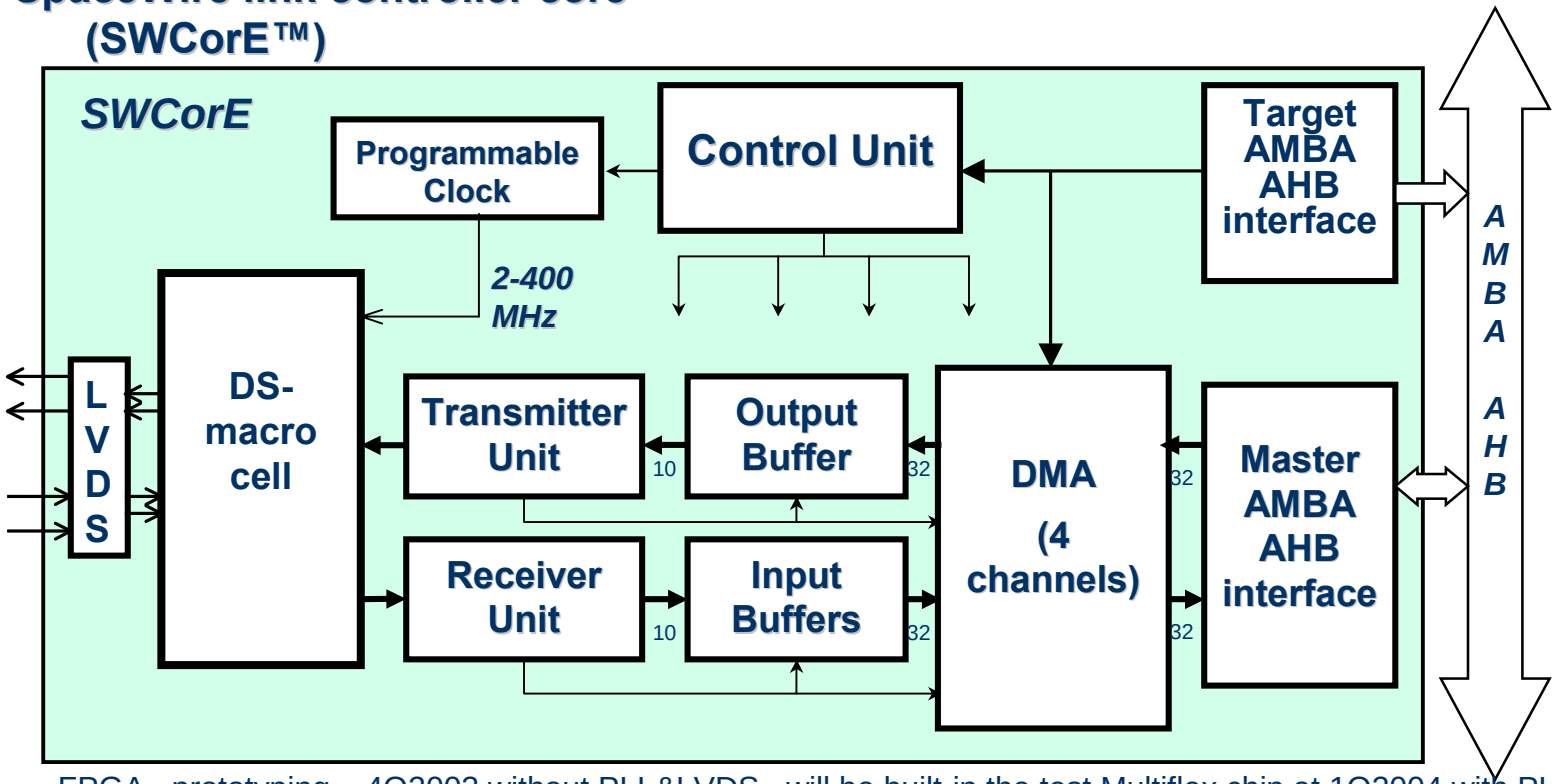
- **Space Wire controller core (SWCorE™)**

- **Special cores:** correlation Core for GPS/GLONASS navigation , DWT, DCT, CORDIC, Viterbi, MP3, special reconfigurable & scalable “ MultiFlex™” cores, Switch Matrix Cores, DAC, ADC…

- **Peripherals Cores**: PCI , USB, UART, I2C, DMA, MPORT…

"MultiCorE™" IP cores library
Space Wire controller core (SWCorE™)

SpaceWire link controller core (SWCorE™)



FPGA –prototyping – 4Q2003 without PLL&LVDS, will be built-in the test Multiflex chip at 1Q2004 with PLL&LVDS

SOC EXAMPLES ON THE BASIS OF THE "MultiCorE" PLATFORM

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GPS/GLONASS - receiver Chip with SMS function

- Peripheral Cores
- System Cores: PLL, DMA, Timer, OnCD
- RISCore _xx
- CORRELATOR Core
- RAM,ROM, CASH, FIFO

Communication modem Chip - MultiCom

- Peripheral Cores
- System Cores: PLL, DMA, Timer, OnCD
- RISCore _xx
- GPS/GLONASS/ COM Cores
- RAM,ROM, CASH, FIFO

3D Graphic chip -MGraph

- Peripheral Cores
- System Cores: PLL, DMA, Timer, OnCD
- RISCore _xx
- OpenGL -Cores
- RAM,ROM, CASH, FIFO

MPEG2 for DTV

- Peripheral Cores
- System Cores: PLL, DMA, Timer, OnCD
- RISCore _xx
- Video Cores
- RAM, ROM, CASH, FIFO

AUDIO INTERNET CHIP

- Peripheral Cores
- ADC/DAC
- System Cores: PLL, DMA, Timer, OnCD
- RISCore_ xx
- DSP
- RAM, ROM, CASH, FIFO

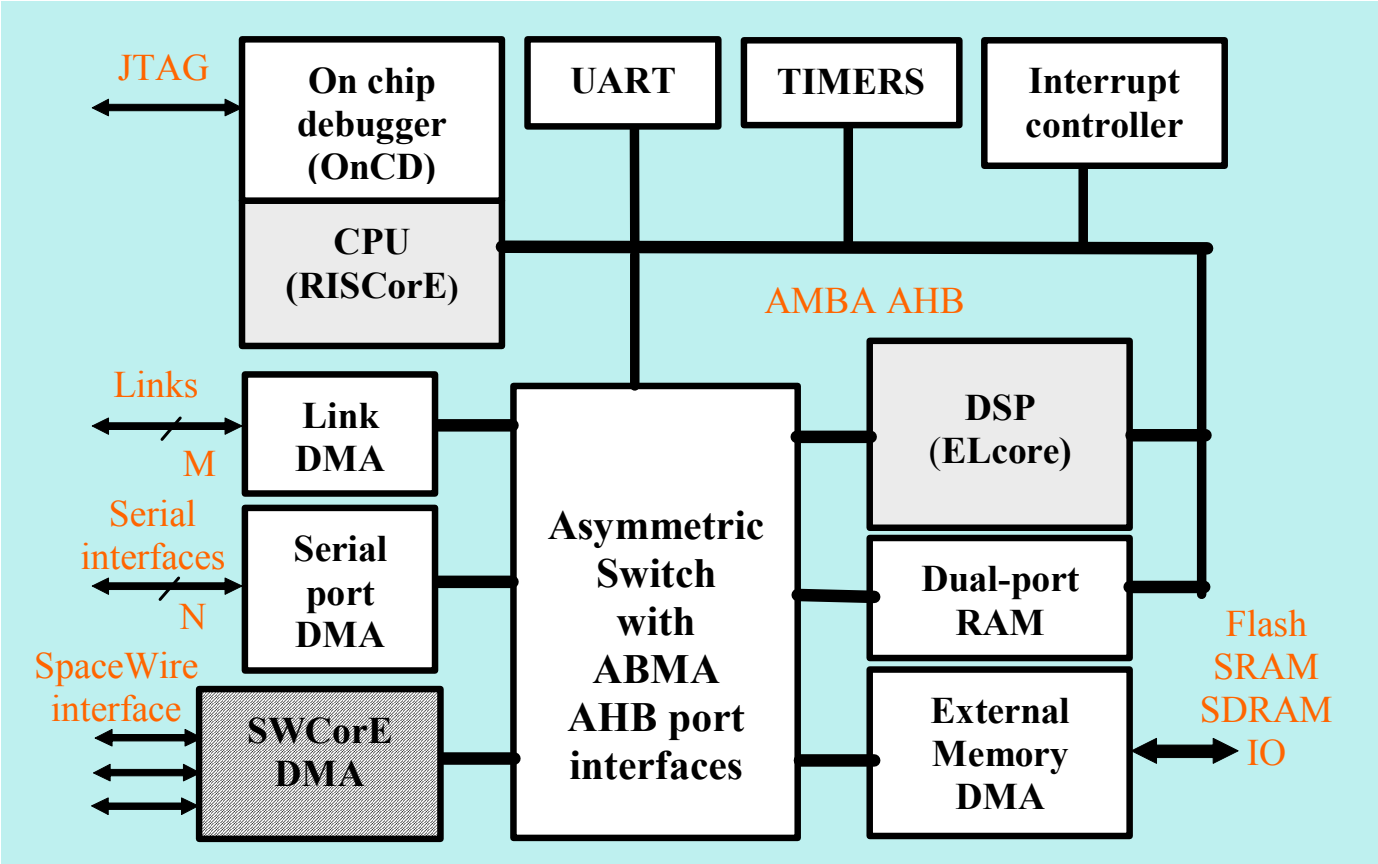
MFlex – DDC/DUC Multistandard transceiver

- Peripheral Cores
- ADC/DAC
- System Cores: PLL, DMA, Timer, OnCD
- RISCore_ xx
- Filters Cores
- RAM, ROM, CASH, FIFO

"MultiCorE™" RISC & DSP IP – cores parameters (preliminary):

Process / Voltage	0.25 µm/2.5 V	0.18 µm/1.8 V
Clock Speed for RISCore_xx/ Floating Point/Fixed Point fast DSP Core (ELcore_14F™), 2-3 Q2004	200 MHz	280 MHz
Clock Speed for RISCore_xx/ Floating Point/ Fixed Point DSP Core (ELcore_14™),1Q2004	100 MHz	140 MHz
GOP/Sec@1-bit Elcore_14F™,~4SIMD	51.2	71.7
GOP/Sec@8-bit Elcore_14F™,~4SIMD:	14.4	20.2
GOP/Sec@16-bit Elcore_14F™,~4SIMD:	6.4	9
GOP/Sec@32-bit Elcore_14F™,~4SIMD:	3.2	4.5
MFLOP/Sec@48-bit (32E16, Extended Floating Point), ELcore_14F™, ~4SIMD:	0.4	0.56
MFLOP/Sec@32-bit (IEEE754), ~4SIMD: ELcore_14™/ ELcore_14F™/	1200/2400	1680/3360
Die DSP- Core Area (max. config. , without memory)	~3.5 mm²	~2.5 mm²

MCFlight™. MultiCore (MC - xxR™) DSC "System –on –Chip" block-diagram.



Kew features of the MultiCore DSC MC - xxR™ (rad hard, preliminary):

- Design rule – CMOS ASIC, 0.25μ & 3.3V (2.5V for core)
- Clock frequency – ~ 70 MHz (for the nominal temperature and voltage)
- On-Chip Memory: ~2Mb
- External memory (managed via memory port) – up to 4Gbytes
- Programmable 32-bit interval timer
- External ports and buses: 3- 6 SpaceWire Links; Four ADI SHARC-compatible byte Links /GPIO, Two ADI SHARC-compatible Serial Ports (SPORTS), UART port, Memory port – External Port for Interfacing to Off-Chip Memory & Peripherals, SDRAM / SRAM / DRAM / Flash ROM "Clueless" System Design, 64-bit data port, 32-bit address port.
- JTAG Test Access and debug port (IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture).
- 16-channel DMA
- Power consumption (3.3V) ~ no more than 2.0 W. Low power dissipation in the idle mode

Some MultiCore (MC - xxR™) peak performance characteristics

Processing data formats: • Fixed point (hardware support) • Floating point (hardware support) • Floating point extended (HW/SW support)	 • 8/16/32 • 24E8 (IEEE 754) • 32E16
Peak performance (for formats): • fixed point, 1b • fixed point, 8b • fixed point, 16b • fixed point, 32b • Floating point (IEEE754) • Floating point extended (32E16)	**Arithmetic op. /1 cycle:** • 128 • 36 • 16 • 9 • 6 • ~0.4
Peak performance (for formats): • fixed point, 1b (MAC: 1*1+32) • fixed point,8b(complex MAC(8+j8)*(8+j8)+32/16) • fixed point, 16b (MAC: 16*16+32) • fixed point, 32b (MAC: 32*32+64) • Floating point (IEEE754) - (MAC: 32*32+32)	**MAC op./1 cycle** • 64 • 4 • 4 • 2 • 2

Dual cores Digital Signal Controller (DSC) MultiCore (R&D Center ELVEES) vs. ADSP- 21160N (ADI)

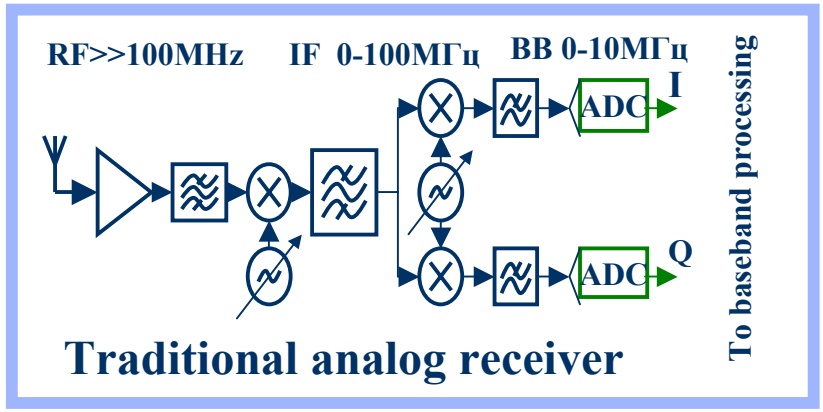
Float point operations, IEEE 754	MultiCore-xxR & 70 MHz 0.25-µm/2.5V core (Rad hard)	MultiCore & 100 MHz 0.25-µm/2.5V core (Not rad hard)	ADSP- 21160N & 95 MHz clock 0.18-µm/1.8V core (Not rad hard)
Peak performance	420 MFLOP/s	600 MFLOP/s	570 MFLOP/s
FFT-1024, complex (radix 4)	151 mcs	106 mcs	97 mcs
Convolution (MAC operation)	140 MMAC/s	200 MMAC/s	190 MMAC/s
FIR Filter (per tap)	7.2 ns	5 ns	5.2 ns
IIR Filter (per biquad section)	29 ns	20 ns	21 ns
Matrix Multiply: [3x3]*[3x1] [4x4]*[4x1]	66 ns 115 ns	46 ns 80 ns	47 ns 83 ns

MCFlight™.
MultiFlex (MFlex-xxR™)

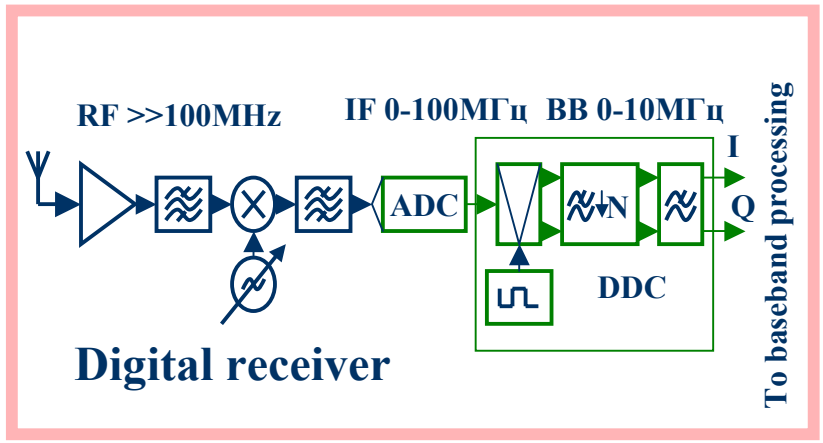
- **MultiFlex (MFlex-xxR™) chips family is a series of single or multi-channel digital down and up converters with scalable architecture**

- **Multi-standard transceiver Chip in ELVEES's MCFlight™ family of customizable SOC chips with SpaceWire links**
and the interface compatibility with DSP chips
- **The application of MultiFLEX gives a great reduction of the analog part complexity** in pre-processing for optical and antenna arrays applications

MCFlight™. MultiFlex (MFlex-xxR™) - DDC (digital down converter) for Soft Radio

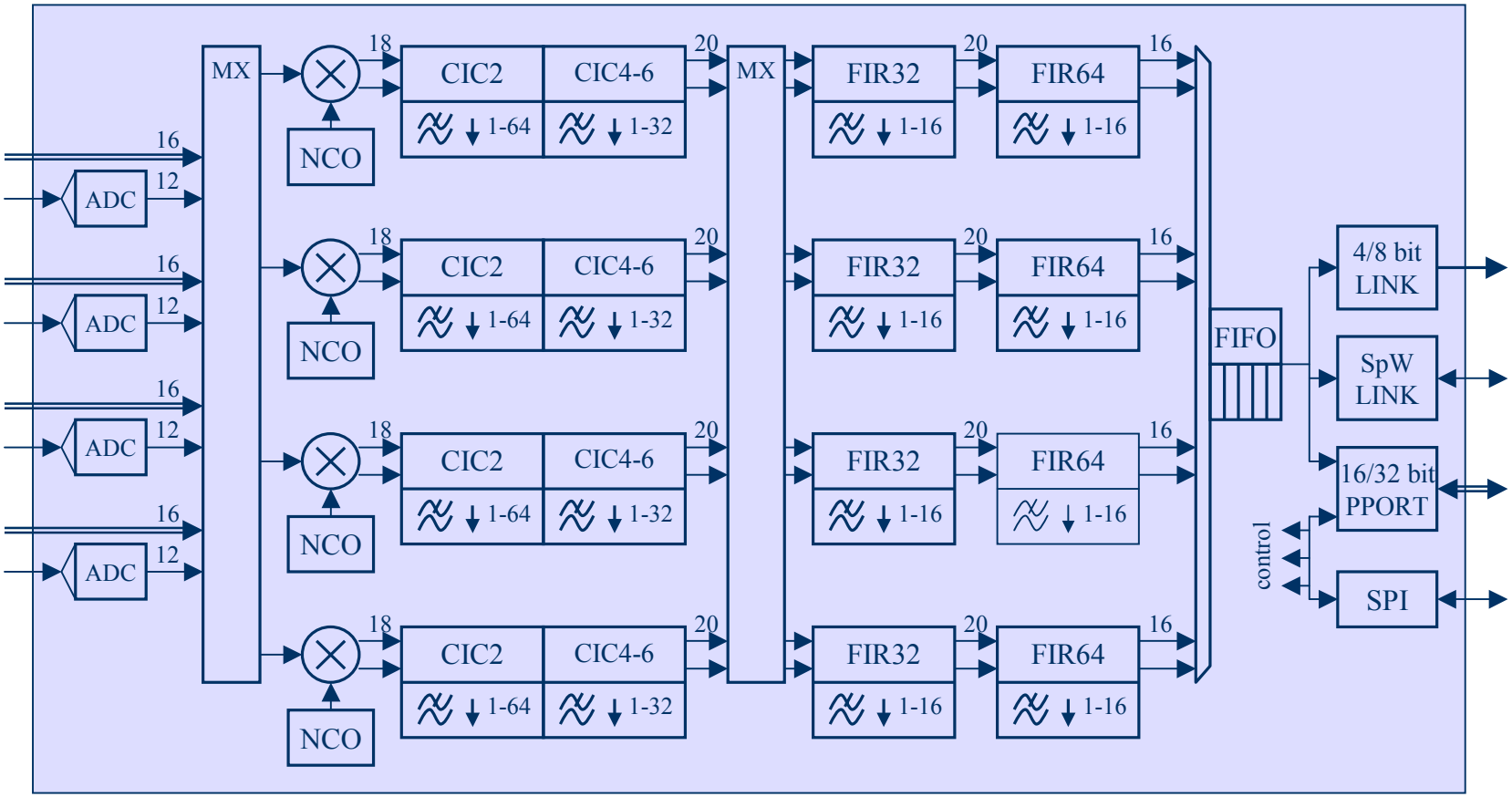


- High accuracy tuning
- High sensitivity to the temperature and component parameters
- Non-linear distortions
- Hard to build filters with rejection below -60Db and reconfigurable filters



- No tuning
- None-sensible to the temperature and component parameters
- Simple implementation of programmable filters with rejection below –100Db
- High accuracy of heterodyne phase and frequency setting

MF01
Four channel digital receiver



MF01 features

Number of DDC channels (narrow/wide)	4/1, Real or complex source signal on intermediate frequency or Baseband
Embedded ADC	4 x12bit, 20MS/s
NCO phase and frequency accuracy:	0.015° / 0.015Hz
Internal datawidht, bits	18
Dynamic range, Db	>105
Input sample rate (external/internal ADC)	80/35
Two stage CIC decimation:	CIC2 and CIC4-6
Two stage FIR decimation and filtering:	32 and 64 TAPs of 1-16 decimation rate each
Output rate for 96 FIR filter:	2.5MS/s for each of four channel, 10MS/s combining all four channels in one
Output data interface:	16/32 bit parallel port, 4/8 bit link port, SpaceWire port
Configuration and control interface:	16/32 bit parallel port, serial port, SpaceWire port
Clock frequency, MHz	80
Effective performance, MMAC/s/GOPs/	~2000/GOPs

MF01(ELVEES) vs. others DDC (ADI&TI)

	MF01	AD6620	AD6634	GC4016
Number of channels	**4**	1	4	**4**
Number of 16-bit inputs	**4**	1	2	3
Embedded ADC	**4**	none	none	none
NCO SFDR, Db	>100	>100	>100	>100
CIC-decimation	CIC2+CIC4-6	CIC2+CIC5	CIC2+CIC5	CIC4
FIR-decimator	**32 TAPs**	None	none	21 **TAPs**
Channel FIR filter	64 (96) TAPs	256 TAPs	160 TAPs	63(84) TAPs
Clock frequency, MHz	80	65	80	80
Throughput for 64-TAP channel filter , MS/s	**2,5**	1	1,25	**2,5**
Effective performance, MMAC	**~2000**	260	~1200	**~2000**

MCFlight™ **Software Development & Debugger Tools**

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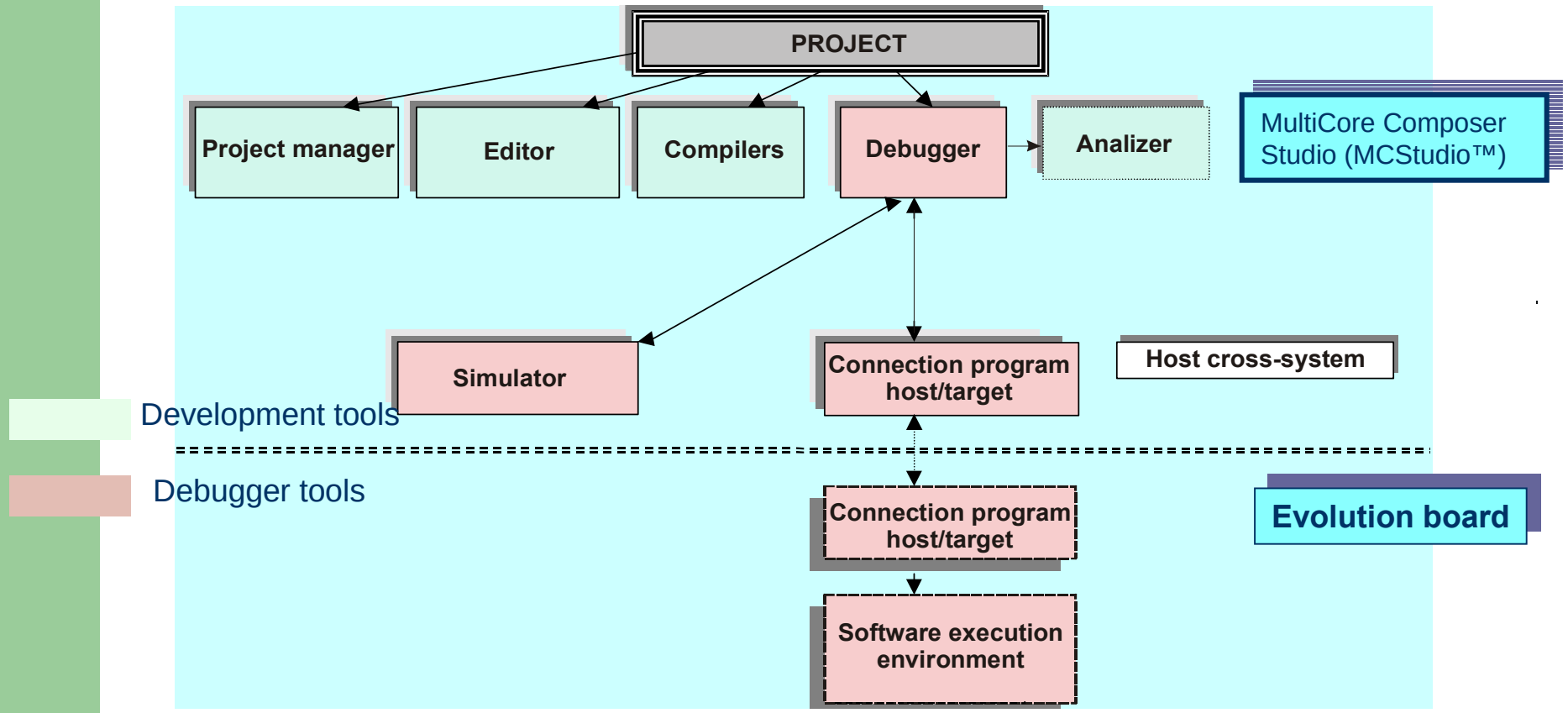
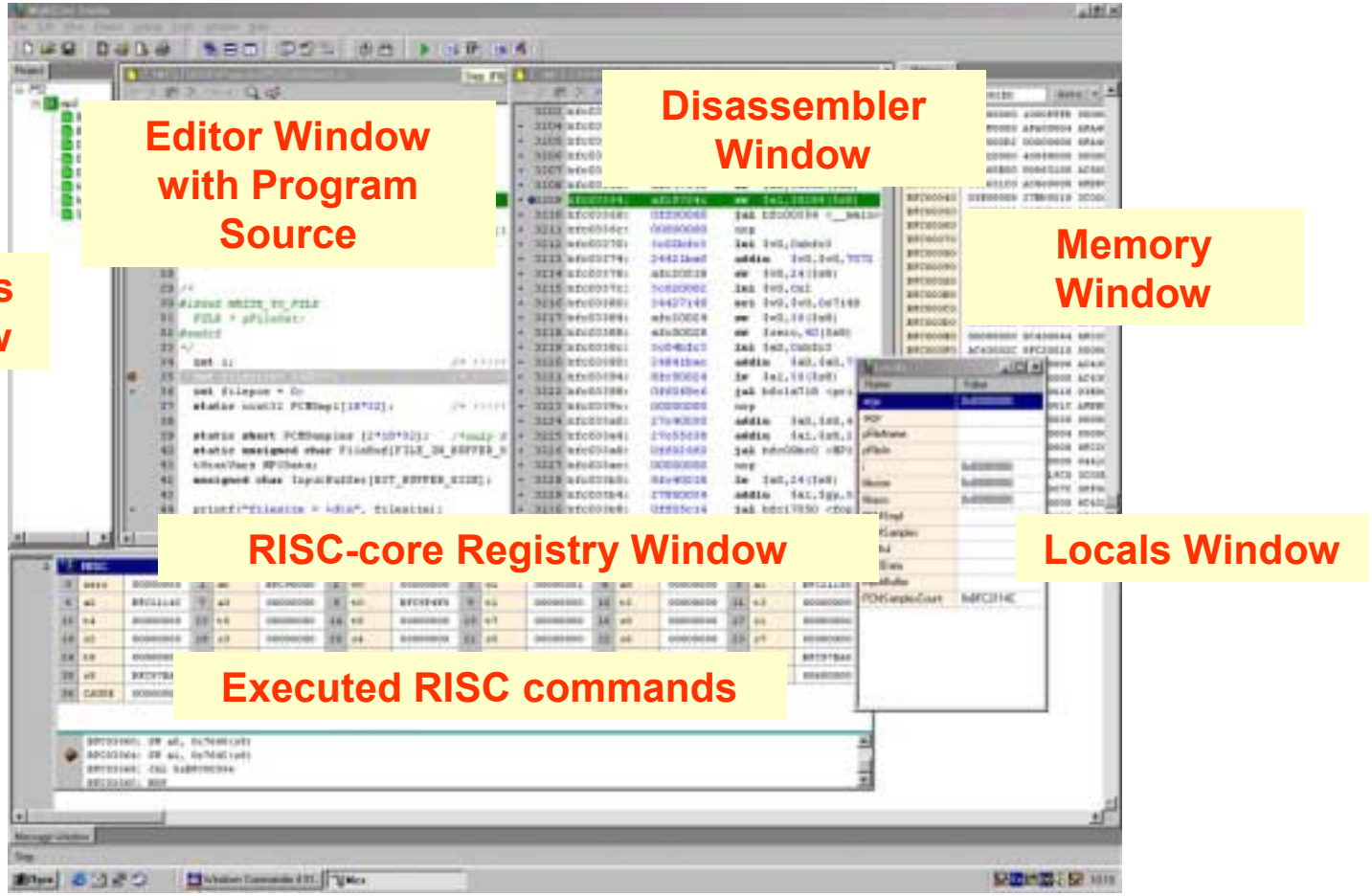


MCFlight™.
Software Development Interface example with open project Windows



MCFlight™ Cores&Chips prototyping and verification technology

2Q2003. PCI Centaurus™ module also **as a part of Software Development Kit for Mflight chipset**

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MCFlight™.
Software Development Kit (ver.2003)

Software Development Kit :

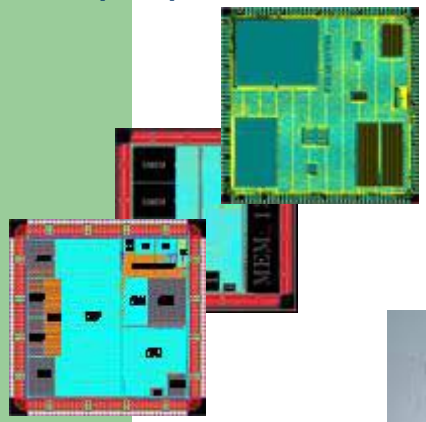
Centaurus Module, OS LINUX, JTAG tools

DSC Evaluation module:

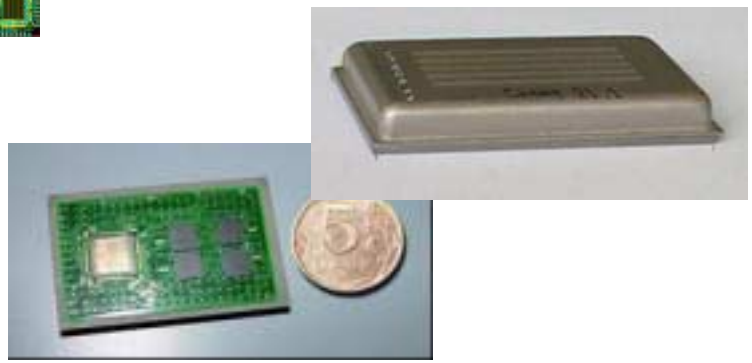
OS LINUX, RTOS, OnCD. JTAG

3 LEVELS of " MCFlight™" utilization for custom specified aerospace systems **(with SpW links in 2004-2005)**:

1st LEVEL - MULTICORE SOC (with SpW)

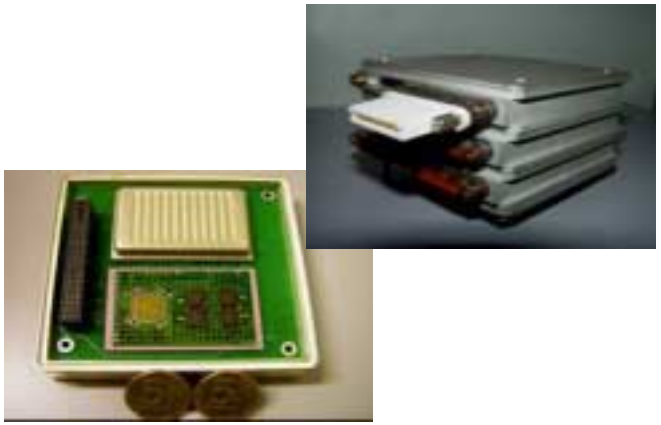


2nd LEVEL – Micro Modul SALUT™ (Multi Chip Micro Modul (MCM) with non-packaged memory chips assembling: 60x40mm*mm, DSC MultiCore test monochip (RISC Core+Float/fixed DSP Core)+512Mb SDRAM +64Mb FLASH). Different kinds of modules with SpW links (with Multiflex chips, SpW Controllers et.)



3rd LEVEL - Unimoduls™

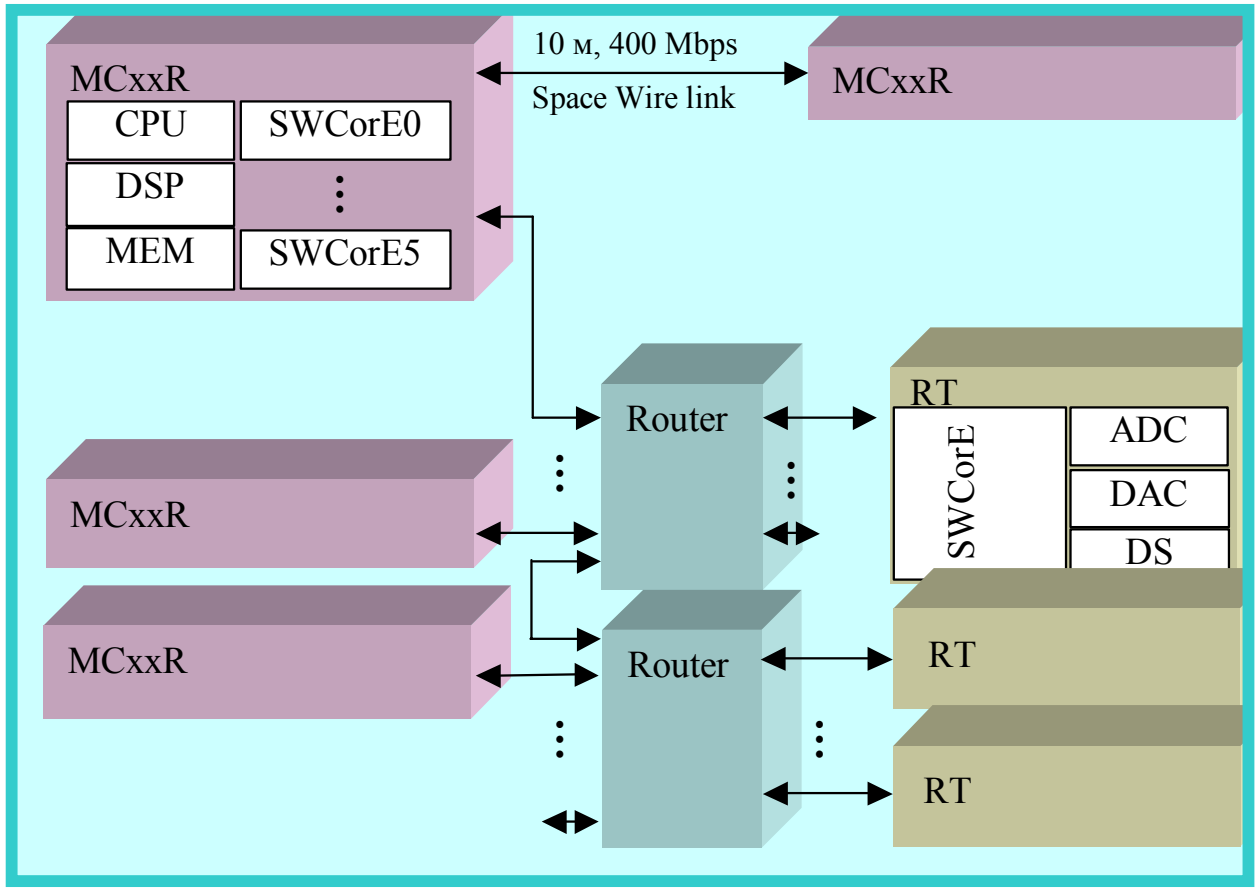
3D stack extended Embedded PC104/Plus boards) – with 2 SALUT MCMs



MCFlight™. **On-board satellite applications (in plans)**

- On-board functional control
- Sensor data processing (including optical/radar), enhancement, compression.
- Satellite's telecommunication: radio modems, soft radio,antenna array digital beam forming for on-board satellite relay

MCFlight™. On-board satellite functional control with adaptive signal processing based on DSC chips (float data format processing & ELVEESs Mflight adaptive algorithms Library)



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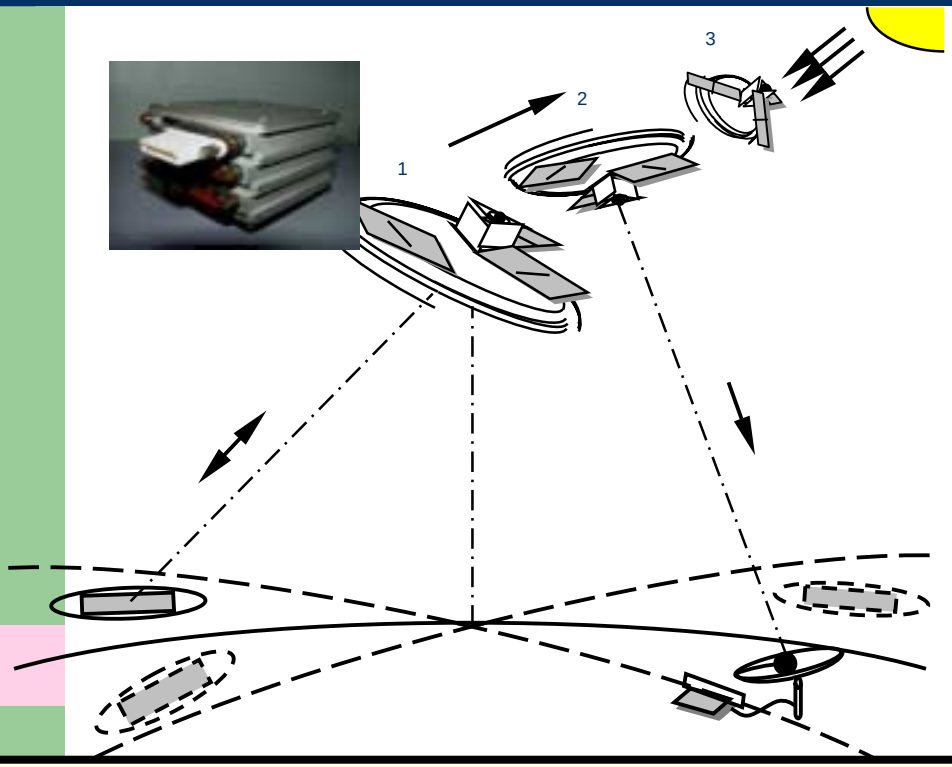
MCFlight™. ELVEES's MCFlight chips based project for small satellite (200kg) with operative ecological on-board radar

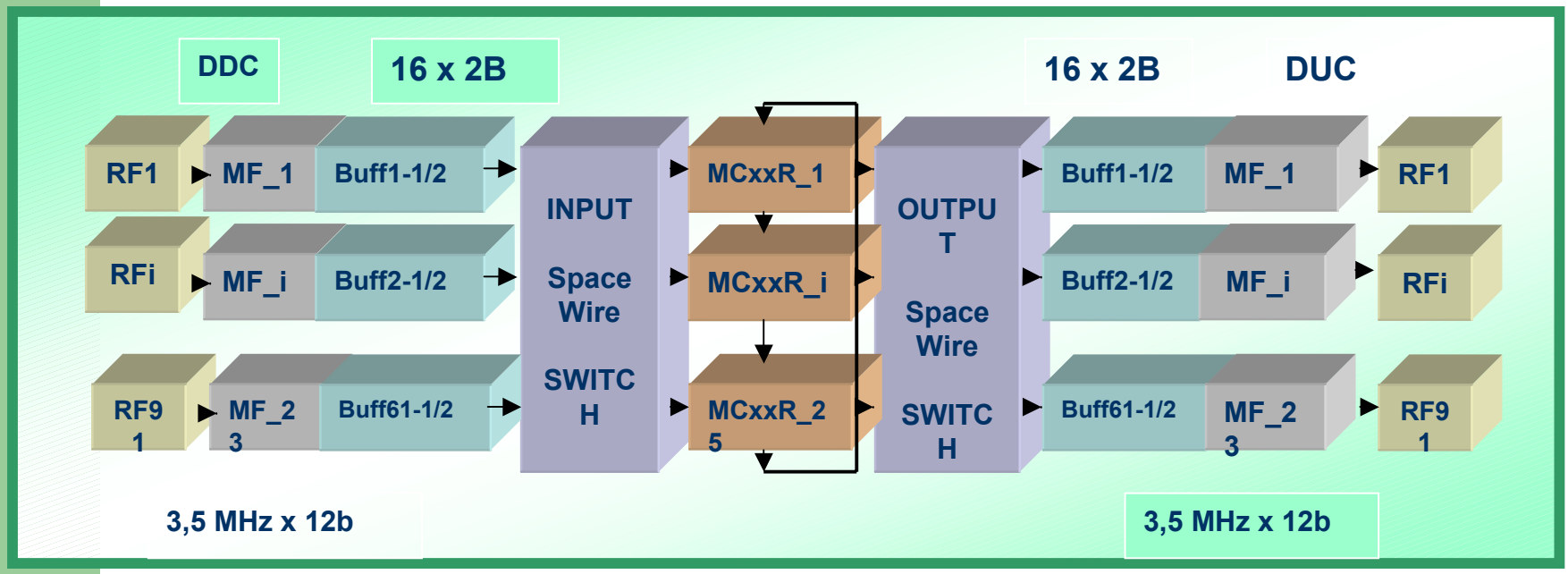


Operating **of the small satellite with** on-board high resolution SAR. **1 -** radar survey**; 2 -** data transmission to the ground terminal**; 3** battery recharge

MCFlight based onboard processor for small satellite high resolution SAR (Synthetic Aperture Radar)

Weight (including SAR antenna) - 250 kg
Linear resolution - 3 meters (grid step 2.5 m)
Frame dimensions - 10 km x 10 km
Looks number (averaging) - 4
Frame survey period - 30 seconds
Processor performance - 8 GOPs
Number of MCxxR chips - 8
Data compression ratio for downlink - min 30 times
Diameter of ground reception station antenna - 1 meter (may be mobile or consumer)
Purpose of system: detailed radar images of natural and artificial origin objects for periodic ecological monitoring

MCFlight™. Example of soft radio, antenna array digital beam forming for on-board satellite relay



System use all types of Mflight Chips:
- Mflex with ADC/DAC & SpW – for preprocessing,
- SpW Switch chips,
- DSC chips –for data processing

Conclusions

Both

✓ELVEESs MCFlight technology on the “System – on – chip level”

✓with ELVEESs MCM and 3D PC104Plus Unimodul

✓together with ESA Space Wire approach on the top system level

can apply really scalable and customizable Distributed Integrated Modular Architecture for Spacecraft On-board Systems, as example, for the telecommunications

Thank for Your attention!

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