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“ELVEES” R&D Microelectronics Center profile:

- was created in 1990 as a part of major in USSA space electronics corporation ELAS;
- in 1974 - the first in the USSA CMOS chip;
- more than 400 successfully developed chips;
- SOC&embedded systems& security
General on-board equipment architecture - integrated architecture systems
SpaceWire based MCFlight™ chipset
ELVEES’s “System - On - a Chip” (SOC) –based open design technology “MultiCorE”
Dual Processors single chip Digital Signal Processors (DSC-RISC-Core+DSPCore) – “MultiCore_xxR” chips
DDC/DUC with build-in ADC/DAC chips for pre-processing – “MultiFlex_xxR” Chips
Tools – “MCStudio”
MCM&Unimodules (PC104plus) on MFlight Chips
MCFlight applications
Distributed Integrated Modular Architecture for Spacecraft On-board Systems
## The MCFlight™ chipset

<table>
<thead>
<tr>
<th>Chips type</th>
<th>Functional purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓ MultiCore (MC - xxR™)</td>
<td>Dual processor (RISC&amp;DSP cores) mooched series of scalable and flexible DSC (Digital Signal Controllers) with SpW Links, 3- 4Q2003 **)</td>
</tr>
<tr>
<td>✓ MultiFlex (MFlex-xxR™)</td>
<td>SDR based DDC/DUC monochip series with SpW Links and built-in ADC/DAC (in plans), 2Q2004 **)</td>
</tr>
<tr>
<td>✓ MCRouter-xxR</td>
<td>Multichannel (16 –channel for 1st realization) Routing switch chip with SpW, 4Q2004 **)</td>
</tr>
<tr>
<td>✓ SWCorE-xxR</td>
<td>Scalable and flexible high performance Serial Communications SpaceWire Controller / Remote-User-Interface ASIC with SpW Links, 3Q2004 **)</td>
</tr>
</tbody>
</table>

*) radiation tolerant (in plans), 0.25μ **) silicon prototyping without radiation tolerant
“MultiCorE™” Platform

Applications

SOC DESIGN TECHNOLOGY

Software Tools

Algorithm

Application Software

HARD

Architecture

IP-CORES LIBRARY

6-9 MONTHLY design flow

TEST Chips examples

ISWS 2003
What are the basic features of the “MultiCorE™” platform?:

- Openness, scalability and flexibility
- 6-9 month's ELVEESs ASIC design flow for SOC integration in Chips
- Multiple processors on the chip (RISC + DSP = DSC – Digital Signal Controller)
- Improved system performance for Digital Signal Controllers (tens GOPs, GFLOPs)
- SW/HW ASIC co-verification on CAD facilities and FPGA prototyping
- Reduced Chip & System Projects development cost and time to market: 3-5 times
- Powerful Tools - MultiCorE Studio (MCStudio™)
The DSC MC_xx series includes:
- MC_11/12/24/01/02/MFlex/MCF-xx...

Key features:
- System integration (multiprocessors, SIMD/MIMD)
- Productivity on the float & fixed point
- Volume of the internal memory
- Presence built-in ADC/DAC, special cores etc.

**DSC mini-configurations**
- MC_11XX and MC_12XX

**DSC maxi-configurations**
- MC_03 and MC_04

**DSC midi-configurations**
- MC_24XX, MC_01XX, MC_02XX

Timeline:
- 2003
- 2004
- 2005

- Mass production
- The project
- Test chip
- In plans
On the basis of MultiCore SoC technology "ELVEES" develops over 10 projects of modern complex multiprocessors monochips simultaneously (also MCFlight chipset with Space Wire Links). Only in 2003 will be developed and made 3 test MultiCore chips: MC-11/12/24 (series in 1Q2004)

Multicore-11T. DSC mini-configurations with the fixed point for built-in applications (test chip - December 2002)

Multicore-24. 2SIMD- configurations
DSC with the amplified fixed point for built in applications (Test chip – Nov. 2003)

Multicore-12. Mini-configurations
DSC, float/fixed point for micro miniature precision embedded applications (Test chip-July 2003)

2.5M transistors & 0.56-mkm & 9.6*9.6 mm*mm:
400MOPs*8b/150MOPs*16b/50MOPs*32b

10M trans.& 0.25-mkm & 9.7*9.7 mm*mm
In a series – 1Q2004:
300MFIOPs/
6400MOPs&1b/
1800MOPs&8b/
800MOPs&16b/
500MOPs&32b
“MultiCorE™” IP Cores library

- Set of similar MIPS32 architecture ELVEES’s RISC - cores (with MAC, without TLB, with FPU, rad hard - RISCorE_xxR™, etceteras)

- Set of 12 float/fixed SIMD scalable ELVEES’s DSP – cores (ELcore_11™/ELcore_12™/ ELcore_13™/ ELcore_14™, etceteras)

- Space Wire controller core (SWCorE™)

- Special cores: correlation Core for GPS/GLONASS navigation, DWT, DCT, CORDIC, Viterbi, MP3, special reconfigurable & scalable “MultiFlex™” cores, Switch Matrix Cores, DAC, ADC…

- Peripherals Cores: PCI, USB, UART, I2C, DMA, MPORT…
“MultiCorE™” IP cores library
Space Wire controller core (SWCorE™)

SpaceWire link controller core (SWCorE™)

FPGA – prototyping – 4Q2003 without PLL & LVDS, will be built-in the test Multiflex chip at 1Q2004 with PLL & LVDS
"MultiCorE™" RISC & DSP IP – cores parameters (preliminary):

<table>
<thead>
<tr>
<th>Process / Voltage</th>
<th>0.25 µm/2.5 V</th>
<th>0.18 µm/1.8 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Speed for RISCore_xx/ Floating Point/Fixed Point fast DSP Core (ELcore_14F™), 2-3 Q2004</td>
<td>200 MHz</td>
<td>280 MHz</td>
</tr>
<tr>
<td>Clock Speed for RISCore_xx/ Floating Point/ Fixed Point DSP Core (ELcore_14™), 1Q2004</td>
<td>100 MHz</td>
<td>140 MHz</td>
</tr>
<tr>
<td>GOP/Sec@1-bit Elcore_14F™, ~4SIMD</td>
<td>51.2</td>
<td>71.7</td>
</tr>
<tr>
<td>GOP/Sec@8-bit Elcore_14F™, ~4SIMD</td>
<td>14.4</td>
<td>20.2</td>
</tr>
<tr>
<td>GOP/Sec@16-bit Elcore_14F™, ~4SIMD</td>
<td>6.4</td>
<td>9</td>
</tr>
<tr>
<td>GOP/Sec@32-bit Elcore_14F™, ~4SIMD</td>
<td>3.2</td>
<td>4.5</td>
</tr>
<tr>
<td>MFLOP/Sec@48-bit (32E16, Extended Floating Point), Elcore_14F™, ~4SIMD</td>
<td>0.4</td>
<td>0.56</td>
</tr>
<tr>
<td>MFLOP/Sec@32-bit (IEEE754), ~4SIMD: ELcore_14™/ ELcore_14F™</td>
<td>1200/2400</td>
<td>1680/3360</td>
</tr>
<tr>
<td>Die DSP- Core Area (max. config., without memory)</td>
<td>~3.5 mm²</td>
<td>~2.5 mm²</td>
</tr>
</tbody>
</table>
Kew features of the MultiCore DSC MC - xxR™ (rad hard, preliminary):

- **Design rule** – CMOS ASIC, 0.25µ & 3.3V (2.5V for core)
- **Clock frequency** – ~ 70 MHz (for the nominal temperature and voltage)
- **On-Chip Memory**: ~2Mb
- **External memory** (managed via memory port) – up to 4Gbytes
- **Programmable 32-bit interval timer**
- **External ports and buses**: 3- 6 SpaceWire Links; Four ADI SHARC-compatible byte Links /GPIO, Two ADI SHARC-compatible Serial Ports (SPORTS), UART port, Memory port – External Port for Interfacing to Off-Chip Memory & Peripherals, SDRAM / SRAM / DRAM / Flash ROM
  “Clueless” System Design, 64-bit data port, 32-bit address port.
- **JTAG Test Access and debug port** (IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture).
- **16-channel DMA**
- **Power consumption (3.3V)** ~ no more than 2.0 W. Low power dissipation in the idle mode
Some MultiCore (MC - xxR™) peak performance characteristics

### Processing data formats:
- Fixed point (hardware support)
- Floating point (hardware support)
- Floating point extended (HW/SW support)

### Peak performance (for formats):
- fixed point, 1b
- fixed point, 8b
- fixed point, 16b
- fixed point, 32b
- Floating point (IEEE754)
- Floating point extended (32E16)

### Arithmetic op. /1 cycle:
- 128
- 36
- 16
- 9
- 6
- ~0.4

### MAC op./1 cycle:
- 64
- 4
Dual cores Digital Signal Controller (DSC) MultiCore (R&D Center ELVEES) vs. ADSP-21160N (ADI)

<table>
<thead>
<tr>
<th>Operation</th>
<th>MultiCore-xxR &amp; 70 MHz 0.25-µm/2.5V core (Rad hard)</th>
<th>MultiCore &amp; 100 MHz 0.25-µm/2.5V core (Not rad hard)</th>
<th>ADSP-21160N &amp; 95 MHz clock 0.18-µm/1.8V core (Not rad hard)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Float point operations, IEEE 754</td>
<td>420 MFLOP/s</td>
<td>600 MFLOP/s</td>
<td>570 MFLOP/s</td>
</tr>
<tr>
<td>Peak performance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FFT-1024, complex (radix 4)</td>
<td>151 mcs</td>
<td>106 mcs</td>
<td>97 mcs</td>
</tr>
<tr>
<td>Convolution (MAC operation)</td>
<td>140 MMAC/s</td>
<td>200 MMAC/s</td>
<td>190 MMAC/s</td>
</tr>
<tr>
<td>FIR Filter (per tap)</td>
<td>7.2 ns</td>
<td>5 ns</td>
<td>5.2 ns</td>
</tr>
<tr>
<td>IIR Filter (per biquad section)</td>
<td>29 ns</td>
<td>20 ns</td>
<td>21 ns</td>
</tr>
<tr>
<td>Matrix Multiply: [3x3]<em>[3x1] [4x4]</em>[4x1]</td>
<td>66 ns 115 ns</td>
<td>46 ns 80 ns</td>
<td>47 ns 83 ns</td>
</tr>
</tbody>
</table>
MultiFlex (MFlex-xxR™) is a series of single or multi-channel digital down and up converters with scalable architecture. It is a multi-standard transceiver chip in ELVEES's MCFlight™ family of customizable SOC chips with SpaceWire links and interface compatibility with DSP chips. The application of MultiFLEX gives a great reduction of the analog part complexity in pre-processing for optical and antenna arrays applications.
To baseband processing

**ADC**

I  Q

IF 0-100 МГц

BB 0-10 МГц

RF >> 100 МГц

Traditional analog receiver

- High accuracy tuning
- High sensitivity to the temperature and component parameters
- Non-linear distortions
- Hard to build filters with rejection below -60Db and reconfigurable filters

**Digital receiver**

- No tuning
- None-sensible to the temperature and component parameters
- Simple implementation of programmable filters with rejection below –100Db
- High accuracy of heterodyne phase and frequency setting

MCFlight™.
MultiFlex (MFlex-xxR™) - DDC (digital down converter) for Soft Radio
MF01
Four channel digital receiver
## MF01 features

<table>
<thead>
<tr>
<th><strong>Number of DDC channels (narrow/wide)</strong></th>
<th>4/1, Real or complex source signal on intermediate frequency or Baseband</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Embedded ADC</strong></td>
<td>4 x12bit, 20MS/s</td>
</tr>
<tr>
<td><strong>NCO phase and frequency accuracy:</strong></td>
<td>0.015° / 0.015Hz</td>
</tr>
<tr>
<td><strong>Internal data width, bits</strong></td>
<td>18</td>
</tr>
<tr>
<td><strong>Dynamic range, Db</strong></td>
<td>&gt;105</td>
</tr>
<tr>
<td><strong>Input sample rate (external/internal ADC)</strong></td>
<td>80/35</td>
</tr>
<tr>
<td><strong>Two stage CIC decimation:</strong></td>
<td>CIC2 and CIC4-6</td>
</tr>
<tr>
<td><strong>Two stage FIR decimation and filtering:</strong></td>
<td>32 and 64 TAPs of 1-16 decimation rate each</td>
</tr>
<tr>
<td><strong>Output rate for 96 FIR filter:</strong></td>
<td>2.5MS/s for each of four channel, 10MS/s combining all four channels in one</td>
</tr>
<tr>
<td><strong>Output data interface:</strong></td>
<td>16/32 bit parallel port, 4/8 bit link port, SpaceWire port</td>
</tr>
<tr>
<td><strong>Configuration and control interface:</strong></td>
<td>16/32 bit parallel port, serial port, SpaceWire port</td>
</tr>
<tr>
<td><strong>Clock frequency, MHz</strong></td>
<td>80</td>
</tr>
<tr>
<td><strong>Effective performance, MMAC/s/GOPs/</strong></td>
<td>~2000/GOPs</td>
</tr>
<tr>
<td></td>
<td>MF01</td>
</tr>
<tr>
<td>------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>Number of channels</td>
<td>4</td>
</tr>
<tr>
<td>Number of 16-bit inputs</td>
<td>4</td>
</tr>
<tr>
<td>Embedded ADC</td>
<td>4</td>
</tr>
<tr>
<td>NCO SFDR, Db</td>
<td>&gt;100</td>
</tr>
<tr>
<td>CIC-decimation</td>
<td>CIC2+CIC4-6</td>
</tr>
<tr>
<td>FIR-decimator</td>
<td>32 TAPs</td>
</tr>
<tr>
<td>Channel FIR filter</td>
<td>64 (96) TAPs</td>
</tr>
<tr>
<td>Clock frequency, MHz</td>
<td>80</td>
</tr>
<tr>
<td>Throughput for 64-TAP channel filter , MS/s</td>
<td>2,5</td>
</tr>
<tr>
<td>Effective performance, MMAC</td>
<td>~2000</td>
</tr>
</tbody>
</table>
MCFlight™ Software Development & Debugger Tools

- Project manager
- Editor
- Compilers
- Debugger
- Analizer
- Simulator
- Connection program host/target
- Host cross-system
- MultiCore Composer Studio (MCStudio™)
- Evolution board
- Software execution environment
MCFlight™. Software Development Interface example with open project Windows
MCFlight™ Cores&Chips prototyping and verification technology

2Q2003. PCI Centaurus™ module also as a part of Software Development Kit for Mflight chipset
MCFlight™. Software Development Kit (ver.2003)

Software Development Kit: Centaurus Module, OS LINUX, JTAG tools

DSC Evaluation module: OS LINUX, RTOS, OnCD. JTAG
3 LEVELS of "MCFlight™" utilization for custom specified aerospace systems (with SpW links in 2004-2005):

1st LEVEL - MULTICORE SOC (with SpW)

2nd LEVEL – Micro Modul SALUT™
(Multi Chip Micro Modul (MCM) with non-packaged memory chips assembling: 60x40mm*mm, DSC MultiCore test monochip (RISC Core+Float/fixed DSP Core)+512Mb SDRAM +64Mb FLASH). Different kinds of modules with SpW links (with Multiflex chips, SpW Controllers et.)

3rd LEVEL - Unimoduls™
3D stack extended Embedded PC104/Plus boards) – with 2 SALUT MCMs
MCFlight™. On-board satellite applications (in plans)

- On-board functional control
- Sensor data processing (including optical/radar), enhancement, compression.
- Satellite’s telecommunication: radio modems, soft radio, antenna array digital beam forming for on-board satellite relay
MCFlight™. On-board satellite functional control with adaptive signal processing based on DSC chips (float data format processing & ELVEESs Mflight adaptive algorithms Library)
MCFlight™. ELVEES’s MCFlight chips based project for small satellite (200kg) with operative ecological on-board radar

- Operating of the small satellite with on-board high resolution SAR. 1 - radar survey; 2 - data transmission to the ground terminal; 3 battery recharge

MCFlight based onboard processor for small satellite high resolution SAR (Synthetic Aperture Radar)

- Weight (including SAR antenna) - 250 kg
- Linear resolution - 3 meters (grid step 2.5 m)
- Frame dimensions - 10 km x 10 km
- Looks number (averaging) - 4
- Frame survey period - 30 seconds
- Processor performance - 8 GOPs
- Number of MCxxR chips - 8
- Data compression ratio for downlink - min 30 times
- Diameter of ground reception station antenna - 1 meter (may be mobile or consumer)

Purpose of system: detailed radar images of natural and artificial origin objects for periodic ecological monitoring
MCFlight™. Example of soft radio, antenna array digital beam forming for on-board satellite relay

System use all types of Mflight Chips:
• Mflex with ADC/DAC & SpW – for preprocessing,
• SpW Switch chips,
• DSC chips – for data processing
Conclusions

Both

✓ ELVEESs MCFlight technology on the “System – on – chip level”
✓ with ELVEESs MCM and 3D PC104Plus Unimodul
✓ together with ESA Space Wire approach on the top system level

can apply really scalable and customizable Distributed Integrated Modular Architecture for Spacecraft On-board Systems, as example, for the telecommunications
Thank for Your attention!

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