HiRel Overview

- Over 30 Years Commitment to the Military and High Reliability IC Industries
- Broad Expanding Product Spectrum
- Broad Process Capability
- Extended Temperature Range
- Baseline Control
- Enhanced Product Change Notification
- Extended Product Life Cycle (Obsolescence Mitigation)
Collaborative Relationships

US Government Liaisons
- US Army
- US Navy
- US Air Force
- NASA
- DSCC
- DMEA
- GIDEP

JC-13 Government Liaison
- JC-13.1 Discrete Devices
- JC-13.2 Microelectronics
- JC-13.4 Rad Hard
- JC-13.5 Hybrids, RF/Microwave, MCM

JC-14 Quality & Reliability

Europe & Asia
- ESA - European Space Agency
- CNES – French Space Agency
- DLR - Deutsches Zentrum für Luft- und Raumfahrt e.V
- BSNC - British National Space Centre
- JAXA - Japan Aerospace Exploration Agency
- DOS/ISRO – India Department of Space & Research
Space Qualified Signal Chain Products

The Real World
- Temperature
- Pressure
- Position
- Speed
- Flow
- Humidity
- Sound
- Light

Signal Conditioning

Power Management
- TPS75003
- TPS703XX
- TPS3809
- TPS40200

Analog to Digital Conversion
- THS4508
- THS4509
- THS4511
- ADS5424
- ADS5444
- ADS5463

Digital Signal Processor
- CDCM7005

Logic & Interface
- AC/ACT
- HC/HCT
- LS
- LVC
- LVT

Digital to Analog Conversion
- THS4513
- THS4304

Timing
- TLK2711
- LVDS31
- LVDS32
- C6701
Programmable DSP is the option of choice for real-time signal processing

- **C62x, C64x**: Highest Performance
  - 8000 MIPS
  - 8000 MACs
- **C67x**: Highest Integration System-On-Chip
  - Portable, Power, Multimedia
  - 1100 MIPS (ARM) + 3200 MIPS (DSP)
- **C5x**: Low Power
- **DaVinci OMAP**: Highest Precision
  - 32/64- Floating Pt
  - 1500 MFLOPS

Real-Time applications are changing the Market.
End Markets

Communication Infrastructure JTRS
Military and Aerospace

Control and Sensing
Military and Aerospace

Multimedia Portable (SDR Handheld)
Public Safety Radios

Homeland security – Video Surveillance
Video Biometrics (Face, Idea & Retina)

Telecom/VOIP/Radio/GPS

Control Applications

C6416/55

C6701/C6727

OMAP™ Devices 642x

DM642 DM6446 OMAP

C5x OMAP

C2x

Increasing Performance, Memory & Peripherals

The HiRel Difference

Technology for Innovators™
Highest Precision
32/64- Floating Point
1500 MFLOPS

C3x, C4x, C67x
Floating-Point DSP HiRel Portfolio

100% Software Compatible

Device
- Production
- Sampling
- In Development
- Future

Increasing Performance

- C31/C32 60 MHz
- VC33 60/75 MHz
- C31 80 MHz
- C6701 167 MHz
- C6711D 167 MHz
- C6712D 167 MHz
- C6713B 200 MHz
- C6713B 200 MHz
- C6727B 300/275 MHz
- C6726B 266 MHz
- C67x+™ Next

1.26V Core
- 0.82W CPU @ 200MHz
- 1.26V Core
- 0.6W CPU
- 1.9V Core
- 1.7W CPU Max
- 2.5W incl. I/O

QML-V, RHA (Planned)
- Ceramic
- Ceramic (Planned)

Technology for Innovators™

Texas Instruments
Highest Performance Floating-Point Digital Signal Processor (DSP) SMV320C6701

- 0.21µ CMOS on Epi
- 7-, 6-ns Instruction Cycle Time
- 140-, 167-MHz Clock Rate
- Eight 32-Bit Instructions/Cycle
- Up to 1 GFLOPS Performance
- 1M-Bit On-Chip SRAM
- 512K-Bit Internal Program/Cache
- 512K-Bit Dual-Access Internal Data
- 32-Bit External Memory Interface (EMIF)
- VelociTI Advanced Very Long Instruction Word (VLIW)

Peripherals
- Two Multi-channel Buffered Serial Ports (McBSP) -- Up to 256 channels each
- Direct interface to T1/E1, MVIP, SCSA framers
- AC-97 and SPI-compatible
- 16-bit HPI

Military Temperature Range: -55°C to 125°C

NOW! - 429 pin CBGA
C6701 Radiation Performance

- High Volume Commercial Process
  - 0.21um (Leff = 0.18um)
  - Added EPI layer
- Total Dose radiation > 100K rad(Si)
  - CO\textsubscript{60} source
- SEU process improvement Available

<table>
<thead>
<tr>
<th>Ions</th>
<th>Incident Angle</th>
<th>LET\textsubscript{eff} (MeV-cm\textsuperscript{2}/mg)</th>
<th>#Units</th>
<th>Test Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ar</td>
<td>0\degree</td>
<td>6.24</td>
<td>1</td>
<td>25\degree C</td>
</tr>
<tr>
<td>Ar</td>
<td>45\degree</td>
<td>9.16</td>
<td>2</td>
<td>25\degree C</td>
</tr>
<tr>
<td>Kr</td>
<td>0\degree</td>
<td>23.6</td>
<td>2</td>
<td>25\degree C</td>
</tr>
<tr>
<td>Kr</td>
<td>45\degree</td>
<td>35.4</td>
<td>2</td>
<td>25\degree C</td>
</tr>
<tr>
<td>Xe</td>
<td>0\degree</td>
<td>47.1</td>
<td>1</td>
<td>25\degree C</td>
</tr>
<tr>
<td>Xe</td>
<td>45\degree</td>
<td>71.1</td>
<td>1</td>
<td>25\degree C</td>
</tr>
<tr>
<td>Xe</td>
<td>45\degree</td>
<td>71.1</td>
<td>3</td>
<td>125\degree C</td>
</tr>
<tr>
<td>Xe</td>
<td>45\degree + #2 Degrader</td>
<td>89</td>
<td>3</td>
<td>125\degree C</td>
</tr>
</tbody>
</table>

Program/Cache and Data Memory
Program Access/Cache Controller and Data Access Controller

Test Data
Weibull Fit

No SEL up to LET of 89 MeV-cm\textsuperscript{2}/mg and max temperature of 125\degree C

SEU Data @ 45\degree
### Summary of SEU Rates (Upsets/day)

<table>
<thead>
<tr>
<th>Environment</th>
<th>EMIF, McBSP, DMA, Power Down Logic, Data Access Controller, Program / Cache Memory, Data Memory, Boot Modes</th>
<th>Program / Cache and Data Memory Program Access/Cache Controller and Data Access Controller</th>
<th>Data Memory Verification using BIST</th>
<th>CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>solar min</td>
<td>4.11E-05</td>
<td>3.32E-04</td>
<td>6.39E-03</td>
<td>7.94E-04</td>
</tr>
<tr>
<td>solar max</td>
<td>9.17E-06</td>
<td>6.83E-05</td>
<td>1.12E-03</td>
<td>1.13E-04</td>
</tr>
<tr>
<td>worst 5-min</td>
<td>3.78E-02</td>
<td>2.44E-01</td>
<td>1.80E-02</td>
<td>5.83E-01</td>
</tr>
<tr>
<td>worst day</td>
<td>3.59E-04</td>
<td>2.43E-03</td>
<td>1.44E-00</td>
<td>5.40E-03</td>
</tr>
<tr>
<td>worst week</td>
<td>1.85E-04</td>
<td>1.42E-03</td>
<td>3.40E-00</td>
<td>3.79E-03</td>
</tr>
</tbody>
</table>

**Estimated worst-case SEU rate of 7.6E-03 upsets/device-day or ~130 days per upset (GEO orbit)**

### Average Anomally Large Solar Flare (ALSF) Upset Rates

<table>
<thead>
<tr>
<th>Environment</th>
<th>Device Upset Rate Upsets/device-day</th>
</tr>
</thead>
<tbody>
<tr>
<td>Worst 5-min</td>
<td>8.83E-01</td>
</tr>
<tr>
<td>Worst day</td>
<td>1.45E-00</td>
</tr>
<tr>
<td>Worst week</td>
<td>3.41E-00</td>
</tr>
</tbody>
</table>
Radiation Tolerance Enhancement

• TI HiRel is actively engaged in R&D to improve the radiation tolerance of CMOS processes for space applications.
  – Non-Invasive Process Technique
    • Boron Backside Blanket Implant
    • 100X SEU Improvement
    • Latch-up Free
# Floating Point DSP Comparison

<table>
<thead>
<tr>
<th></th>
<th>C6701B 167 MHz</th>
<th>C6713B 200 MHz</th>
<th>C6727 250 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MIPS MFLOPs</strong></td>
<td>167 x8= 1336</td>
<td>1600</td>
<td>2000</td>
</tr>
<tr>
<td></td>
<td>1000</td>
<td>1200</td>
<td>1500</td>
</tr>
<tr>
<td><strong>Architecture</strong></td>
<td>C67x</td>
<td>C67x</td>
<td>C67x+</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>64KB Data Memory</td>
<td>4KB L1-P, 4KB L1-D, 256KB L2 Cache/SRAM</td>
<td>32KB L1-P, 256KB L2 SRAM, 384KB ROM</td>
</tr>
<tr>
<td></td>
<td>64KB Program Memory</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>HPI</strong></td>
<td>HPI-16</td>
<td>1 32/16-bit</td>
<td>1 UHPI 32/16-bit</td>
</tr>
<tr>
<td><strong>EMIF</strong></td>
<td>100MHz 32-bit (SDRAM)</td>
<td>100MHz 32-bit (SDRAM)</td>
<td>100MHz 32-bit (SDRAM)</td>
</tr>
<tr>
<td><strong>DMA</strong></td>
<td>4-ch DMA</td>
<td>16-ch EDMA</td>
<td>16-ch dMAX</td>
</tr>
<tr>
<td><strong>McBSP</strong></td>
<td>2</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td><strong>McASP</strong></td>
<td>0</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td><strong>I2C</strong></td>
<td>0</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td><strong>SPI</strong></td>
<td>0</td>
<td>0</td>
<td>2 (10MHz)</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td>429-pin Ceramic BGA (27mm, 1.27mm)</td>
<td>272-pin PBGA 27x27xmm, 1.27mm (Ceramic Package TBD)</td>
<td>256-pin PBGA 16x16mm, 1.0mm (Ceramic Package TBD)</td>
</tr>
</tbody>
</table>

Software Compatible
C6713B DSP

**Features**

- **C67x™ Core**
  - Memory
    - 264 KBytes On-Chip Memory
    - 4 KBytes L1P / 4 KBytes L1D
  - **Peripherals**
    - Two Multi-channel Audio Serial Ports (McASP)
      - Up to 16 stereo channels of IIS
      - Up to four different clock rates
      - Compatible with S/PDIF transmit protocol
    - Two I²C Ports
    - Two Multi-channel Buffered Serial Ports (McBSP)
      - Up to 256 channels each
      - Direct interface to T1/E1, MVIP, SCSA framers
    - 32-bit EMIF; 16-bit HPI

- **Package:** Ceramic package (Planned)

![Diagram of C6713B DSP architecture](image-url)
C6727B DSP
Highest-Performance Floating-Point Processor

Features

- **New C67x+™ DSP Core**
  - 275/300 MHz; 1650/1800 MFLOPS

- **Memory**
  - 256 KB of SRAM and 32 KB of I-Cache
  - DSP/BIOS™/DSPLIB/FastRTS Library included in the device

- **Peripherals**
  - 32-bit HPI for Connecting to Hosts
  - dMAX Support for 1D, 2D, 3D Transfers as well as Multi-Tap Memory Delay
  - Three McASPs
  - Two I²C, two SPIs, 133 MHz/32-bit EMIF

- Ceramic Package (Planned)

EVM Available
C672x™ Improvements

Significant Overall Increase in CPU Performance

- Number of CPU registers doubled to 64
- Instruction cache increased from 4kB to 32kB
- Flat memory model for Data
- Doubled the simultaneous floating-point additions.
- New accuracy instructions
  - SP * DP → DP, SP * SP → DP
- Code size reduction
  - Execution packets can span fetch packets (Like C64x DSP)
- dMAX : New DMA engine

Together, >25% lift in performance.
Low Power C2x Family
C2000 DSP Hi-Rel Portfolio

High-Precision Uni-processor Control for Applications from Industrial Drives to Automotive

Device
- Production
- Sampling
- In Development
- Future

Multi-Function, Appliance & Consumer Control

C2000 DSP Hi-Rel Portfolio

F283xx
- Commercial samples 2Q07
  - 16Kx2B Flash
  - 32Kx2B Flash
- Ceramic
- QML-V Release planned for C2812

F2808
- QFP/u*BGA
- 32-bit &100 MIPS
- 16Kx2B Flash
- 6.25 MSPS 12-bit ADC

F2801
- 32-bit &150 MIPS
- 128Kx2B Flash
- 16-ch 12.5 MSPS 12-bit ADC

F2812
- 32-bit &150 MIPS
- 128Kx2B Flash
- 16-ch 12.5 MSPS 12-bit ADC

F2407
- 40 MHz
- 32Kx2B Flash
- 16-bit
- 40 MIPS
- 10-bit ADC

F240x
- 40 MHz
- 16Kx2B Flash
- 16-bit
- 40 MIPS
- 10-bit ADC

Non-Flash version planned for QML-V,RHA

Future

High-end F28x

Ceramic

Production

Sampling

In Development

Future

Technology for Innovators

Texas Instruments
F2812: A Complete System-on-a-Chip

Memory Sub-System

- 4X larger Flash Memory
- Fast program execution out of both RAM and Flash memory
- 128-bit security provides on-board software security
- External memory interface (XINTF) supports systems with larger memory models (up to 1Mw address reach)

Control Peripherals

- Event Managers optimized for motor control and power conversion applications
- Fast & Flexible 12-bit ADC critical in completing analog control loops
- Up to 60 general purpose I/O pins can be used for controlling relays, LED’s, reading switches, etc.

Communications Ports

- Multiple standard communication ports provide simple communications interfaces to other components
- CAN controller is 2.0B compliant and provides a glueless interface to CAN networks for a variety of applications
F283xx – The Industry’s First Floating-point Digital Signal Controllers

50% performance boost
Floating-point unit boosts performance by an average of 50% over today’s highest performance digital signal controllers

Simpler software development with floating point
Save months by avoiding conversion to fixed point

Lower overall system cost
Single-chip solution for high-performance industrial control applications
F2833x Digital Signal Controllers

**Processor Performance**
- 300 MFLOPS at 150MHz
- Single-cycle 32-bit MAC
- 6-channel DMA support for EMIF, ADC, McBSP

**Memory**
- Three memory options with up to 512KB flash and 68KB RAM
- Configurable 16- or 32-bit EMIF

**Control Peripherals**
- PWM outputs interfaces for three 3-phase motors
- 6 High-resolution PWM outputs
- Highest-speed on-chip ADC

**Communications Ports**
- Each McBSP configurable as SPI
- CAN 2.0b with 32 mailboxes
- I²C at 400 Kbps

**Development Tools**
- F28335 eZdsp kit (coming in October)
- Code Composer Studio™ IDE
- Software libraries
Foundry Technology & Product Portfolio

EDA\CAD TOOL SUPPORT

LinBiCMOS  BiCMOS - RF  Analog  Feature size  CMOS Low power  CMOS High Performance

Virtuoso Composer  CDS NC  Virtuoso Layout Editor  HDL Text Editor  Design Compilers
RTI Complier  Spectre  K2 Chameleon (VER)  TISpice  BlastRTL  Power Compilers
Virtuoso XL Layout Editor  UltraSim  Assura DRC/LVS/RCX  Analog Circuit Studio  BlastFusion
VDIO / Nano Encounter  UltraSim  Assura DRC/LVS/RCX  HVAL Utils  Tetramax

Texas Instruments
Summary

Current Environment:

• TI C6701 is the highest performance floating point DSP in the Space market with 100k Rad (Si) TID
  – TI considering additional non-invasive radiation performance improvements and welcomes partners for these efforts

Future Plan:

• TI C6727 is the next high performance DSP targeted for the Space applications. Product qualification timing is customer / market driven
  – Also on the roadmap are C28xx & C283xx families (customer driven)

• Please let us know how can become part of your signal chain solution!

Note:
Under the jurisdiction of the US Dept of Commerce, all Catalog TI DSPs operating in full mil temp range of -55C to 125C are controlled under Export Control classification of 3A001A2C
THANK YOU